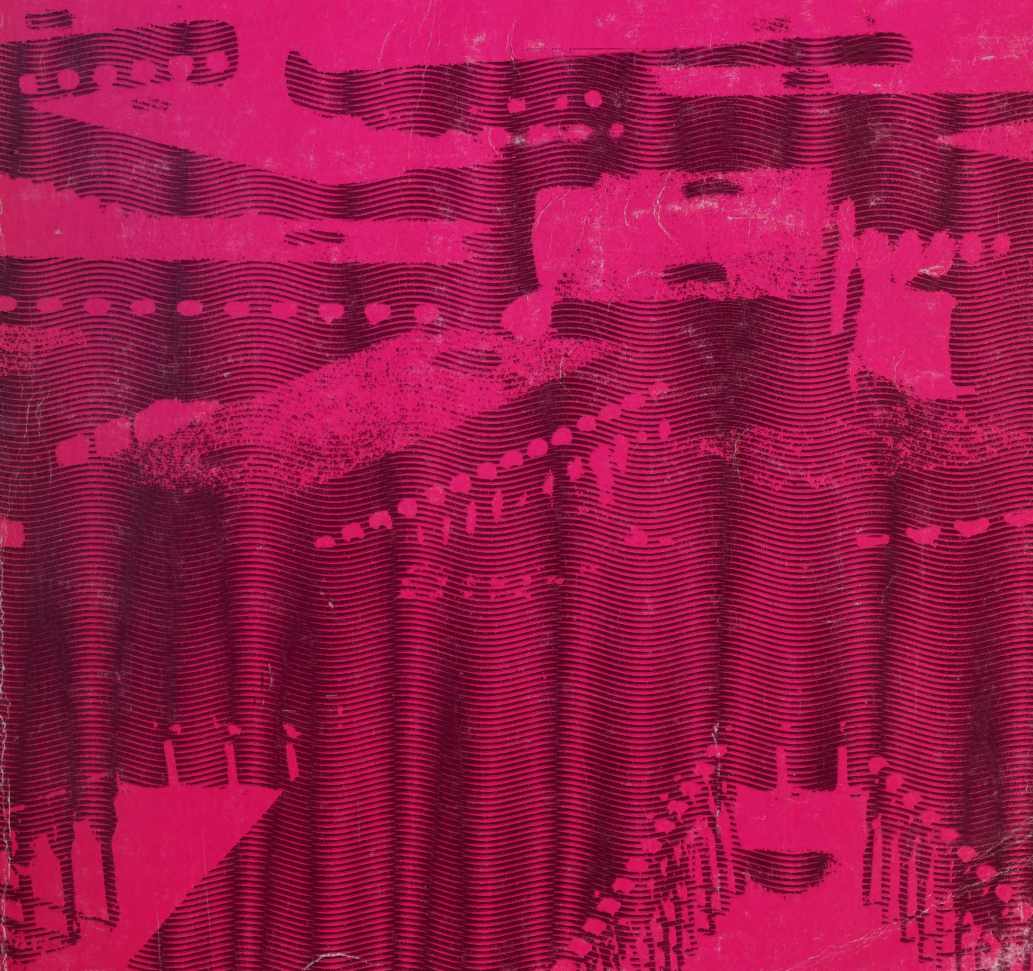
MARCH 1985

SATELLITE CABLE AND TV INTEGRATED CIRCUIT HANDBOOK

PLESSEY
Semiconductors



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Designed and produced by Peter Wigens Consultants
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EXP Products

Products in this Handbook that have the suffix EXP after their type numbers are new products designated 'Experimental' but which are, nevertheless, serious development projects. Details given may, therefore, change without notice and no undertaking is given or implied as to future availability. Please consult your local Plessey Semiconductors Ltd. sales office for details of the current status.

SP4000 Series

The SP4000 series of low-current, low-radiation prescalers for TV tuners is constantly expanding to meet the requirements of the industry. Many of these products are included in this handbook; further information, particularly additions to the series, is published separately in the *Low-Current, Low-Radiation Prescalers* brochure, available from Plessey Semiconductors on request.

Selection guide

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SL1451	Wideband PLL FM detector for satellite TV	135
SL1452	1GHz wideband FM detector for satellite TV	137
SP5050EXP	1.8GHz PLL tuning controller	229
SP5051EXP	2.0GHz PLL tuning controller	229
SP5060EXP	1.8/2GHz single chip frequency synthesiser	235
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SL1430	Ultra linear preamplifier, 22dB gain 100MHz, differential O/P optimised for driving surface acoustic wave filters	127
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MR9710	Data acquisition	57
MR9735	Video generator, 625 lines, interlaced/non-interlaced	65
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Quality data

Plessey Semiconductors has Factory Approval to:-

BS9300 for semiconductor devices of Assessed Quality (BSI Certificate 1053/M)

BS9400 for integrated circuits of Assessed Quality (BSI Certificate 1053/M)

CECC 50000 Inspection Organisation to document level 1 (BS9300) M0020/CECC refers

DEF STAN 05— 21 QC System requirements for Industry (Equivalent to AQAP— 1) Certificate 65752/1/01 refers

DELIVERED PRODUCT QUALITY

It is our policy to deliver a relaible quality product and to achieve this end all devices undergo 100 % electrical testing of every relevant AC and DC parameter prior to shipment. The devices are tested under conditions of level and frequency closely simulating those of the typical application. Fully automatic Teradyne integrated circuit test machines, acknowledged to be among the best computer controlled test machines available, are employed.

Each and every stage of processing, assembly and testing is carefully audited by Plessey Semiconductors' independent Quality Assurance department.

Therefore we are able to guarantee the following Acceptable Quality Level (A.Q.L.) on all deliveries.

MECHANICAL

Defects of a mechanical nature including coding not being legible, deformed leads, dimensional tolerances being exceeded, wrong identification of pin 1 and pins not being solderable.

0.65 % AQL, I.L.II

ELECTRICAL

Defects of an electrical nature including device parameters being outside the acceptance specification limits, or those only stated as typical being grossly in error.

0.4 % AQL, I.L.II

The average delivered product quality is considerably better than this, the population of imperfect devices being much smaller than that indicated by the AQL values.

Semi-Custom

For Semi-Custom to be effective, the customer must have available to him a whole range of high performance technologies and design techniques.

Technologies to match current requirements and continuing development to ensure his planned products maintain their market lead.

The table below outlines Plessey Semiconductors' current selection.

Microcell

MJ1000 5 micron NMOS Up to 3000 equivalent gates

Microgate-C

CLA2000 5 micron Silicon Gate CMOS 840 - 2400 gates Gate Delay 3.5ns typ.

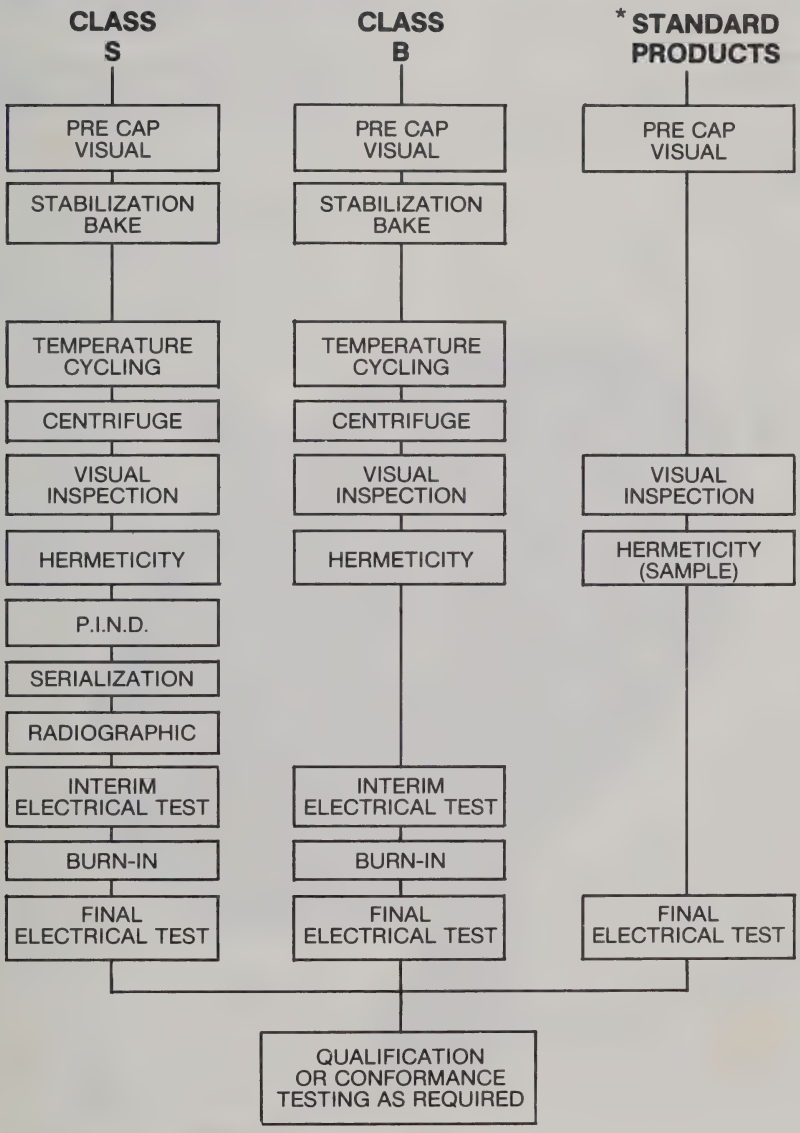
CLA3000 4 micron Silicon Gate CMOS 840 - 420 gates Gate Delay 2.5ns typ.

CLA5000 2 micron Silicon Gate CMOS 640 - 10440 gates Gate Delay 1.2ns typ.

(Gate delays given are for 2 input NAND)

Screening

The following Screening Procedures are available from Plessey Semiconductors



*Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

PLESSEY ICs for Satellite Reception

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PLESSEY ICs for Satellite Reception

Plessey Semiconductors are one of the world's leading suppliers of high frequency Integrated Circuits. Our long experience in supplying high performance high quality circuits for military applications together with our experience in supplying high volume products to the cable TV and broadcast TV manufacturing industry has put us in a strong position to supply the newly emerging Satellite Reception market.

To enable manufacturers to design and produce Satellite Receiver Equipment in time for this potentially very large market, Plessey Semiconductors have brought together their expertise to produce the key IC s required.

Typical Satellite Receiver System

The outddor unit mixes the incoming 4 or 12GHz signal down to 950-1450MHz. This is achieved by multiplying an oscillator controlled by Plessey's SP5060 PLL. After mixing the resultant signal is buffered and sent down a coax link to the indoor unit.

The signal is amplified at the indoor unit after passing through a wideband filter. This amplifier may incorporate AGC to provide the optimum signal level for the mixer and subsequent stages. The required signal is selected from the band by mixing with the output from a PLL controlled oscillator using Plessey's SP5051 and converted to a second IF of between 380MHz - 650MHz.

Some full band systems may require the PLL to operate above 2GHz. In this case a prescaler such as the Plessey SP8712 which provides ÷4 at up to 2.4GHz will be required.

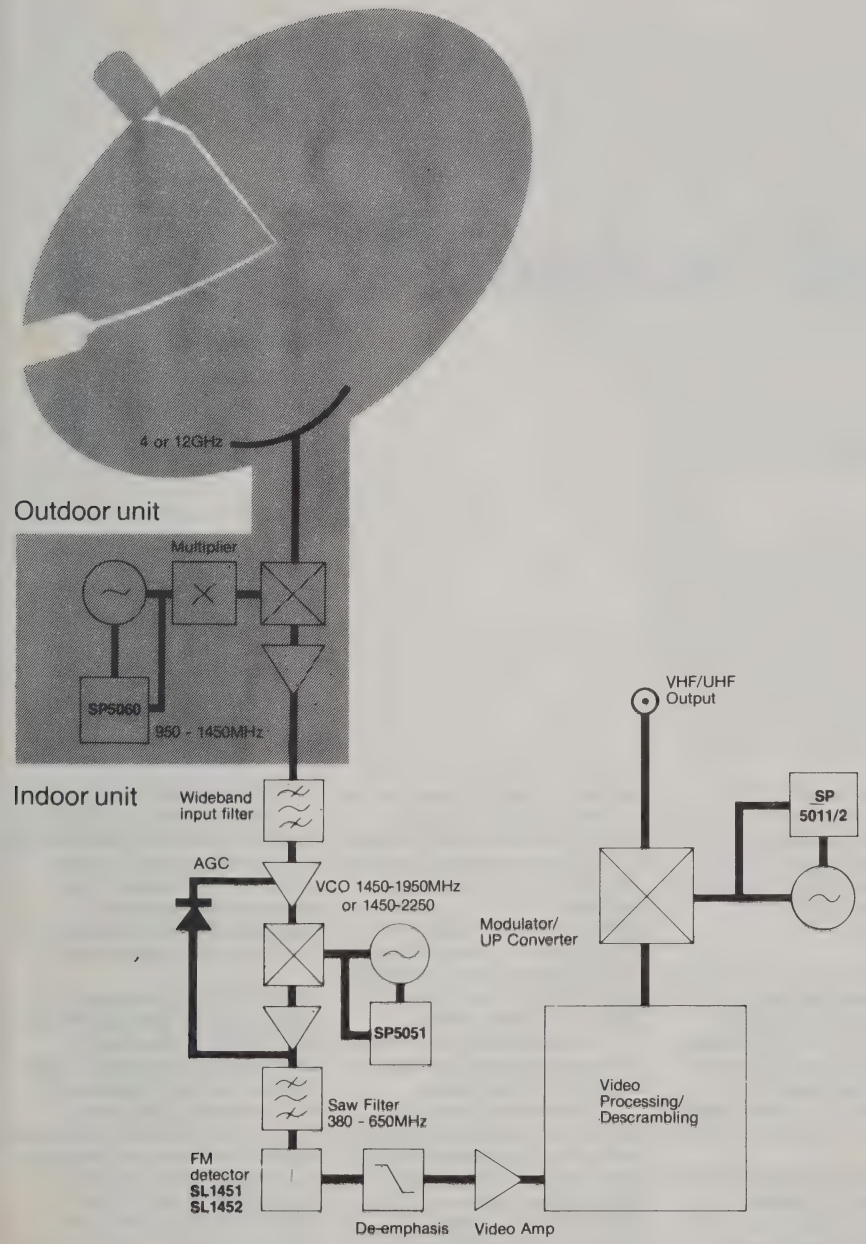
The high second IF greatly simplifies design problems by placing the image at a point which obviates the need for tracking filters.

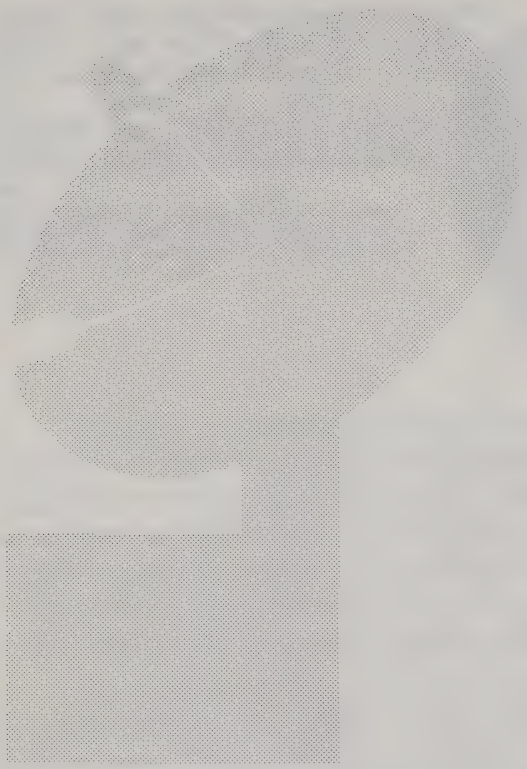
After mixing, the signal passes through another amplifier to make up the losses of the following SAW filter. The AGC feedback signal is also detected at this point.

After passing through the SAW filter which must be capable of passing the FM signal without loss of information, detection is performed by one of the Plessey FM detectors. These devices can operate at frequencies well above the highest common IF of 612.75MHz with minimal signal distortion and give excellent threshold performance.

The detected signal will then be decoded and descrambled as required. Here Plessey can offer its long experience in CCD technology and Semi-custom design in Bipolar and CMOS technology.

Finally the signal will be converted up to a suitable channel for connection to the standard TV input using an SP5011 or SP5012 to give accurate PLL control of the frequency with a number of alternative options.


4 or 12GHz
Outdoor unit
Multiplier
SP5060
950 - 1450MHz
Indoor unit
Wideband
input filter
AGC
VCO 1450-1950MHz
or 1450-2250
SP5051
Saw Filter
380 - 650MHz
FM
detector
SL1451
SL1452
De-emphasis
Video Amp
VHF/UHF
Output
SP
5011/2
Modulator/
UP Converter
Video
Processing/
Descrambling



Technical Specification

SL1451 This is a PLL FM wideband detector, designed for satellite receivers employing an IF of 380 to 700MHz. This device gives threshold extension for improved system performance.

SL1452 This is an FM wideband Detector designed to operate in satellite reception systems employing high IF of between 400-1000MHz. Using a high IF eliminates the need for a tracking filter for Image rejection and so greatly simplifies system design.

The other advantage is that the deviation is a small percentage of the IF and very good linearity is achieved.

SP5060 This is a PLL for use in the outdoor (head end) unit. It needs no microprocessor but can synthesise any frequency in the range 500MHz to 1.8GHz by appropriate choice of reference frequency. This, together with a frequency doubling mixer, enables C-Band (4GHz) signals to be block-converted down to a standard first IF of 950MHz to 1450MHz.

SP5050/1 The SP5050/1 are single chip PLL controllers. The SP5050 offers 50mV sensitivity at 1.8GHz and the SP5051 is a 100mV, 2.0GHz device.

These devices can be used to control the local oscillator of the second mixer stage.

The required channel is selected at the second stage by mixing the signal down to an IF which will usually be 480MHz for European systems and 510MHz or 612.75MHz for USA/Canadian systems. The SP5050/1 are controlled by a 16 bit word from a 4 or 8 bit micro which gives 125kHz steps over the range.

Since the oscillator runs higher than the incoming signal, full band systems could require a PLL to operate up to 2.4GHz.

Plessey offer a ÷4 SP8712 together with a standard SP5000 PLL to achieve this. Further prescaler options with high prescaler ratios are in development for this top end of the frequency requirement.

SP5011/2 Fixed frequency versions of the original SP5000 PLL controller needing no micro-processor control. These devices give eight options of PLL controlled frequency conversion. They can be used to convert the baseband signal up to a UHF or VHF channel for connection to the TV or conversion from VHF cable frequencies up to UHF or higher VHF channels.

Amplifiers Plessey produce a range of high frequency amplifiers which is being further extended to 2GHz for Satellite Reception systems.

Technical Data

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ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

CT2200

5-BIT BINARY TO 13-SEGMENT DECODER/DRIVER

The CT2200 is an N-channel MOS integrated circuit, designed to directly drive two 7-segment LEDs to display the numbers 1 to 32, with leading zeros suppressed. The circuit is ideal for applications such as the programme number display of a television receiver. The display is controlled by a 5-bit binary input port, weighted so that the number shown (1-32) is one more than the binary input (0-31) to avoid programme 0. The 5 lines can come from a remote control receiver or from any other source of continuous 5-bit data.

Common anode LEDs can be driven directly with a current limiting resistor in series with each output (see Fig.5) or by using some other form of brightness control (see Fig.6). By driving each segment individually the interference problems associated with multiplexed displays are avoided.

A blanking input is provided so that the display can be turned off or can be made to flash with an external pulsed signal.

Only 13 lines are needed for two 7-segment displays because segment Tf is never lit for the numbers 1 to 32 and so does not need to be decoded and driven. Segment identification is shown in Fig.2.

The 13 outputs of the output encoder drive the gates of large output transistors to give two states: OFF and SINK CURRENT; as there can be up to 12 outputs on at once, each sinking 20mA, four 0V pins are provided to reliably carry this current. **ALL FOUR PINS (3, 7, 18, 22) MUST BE CONNECTED TO 0V.**

The number of segments required for each character is shown in Fig.3.

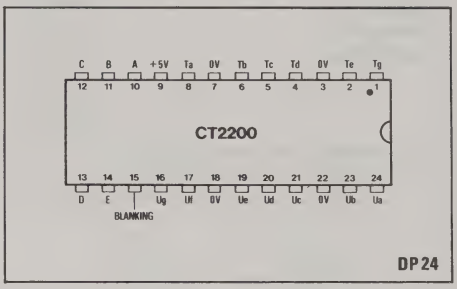

Fig.1 Pin connections - top view

FEATURES

- Direct Segment Drive — Non-Multiplexed
- 5V Supply
- Blanking Input
- Leading Zero Suppressed
- Minimum Segment Pattern per Character
- 20mA Drive per Segment
- 5-Bit Binary Input

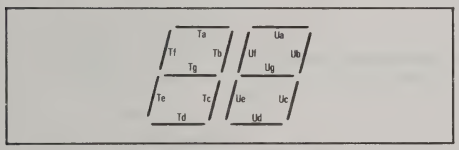

Fig.2 Segment identification

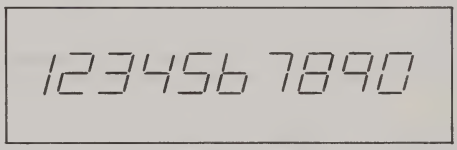

Fig.3 Character representation

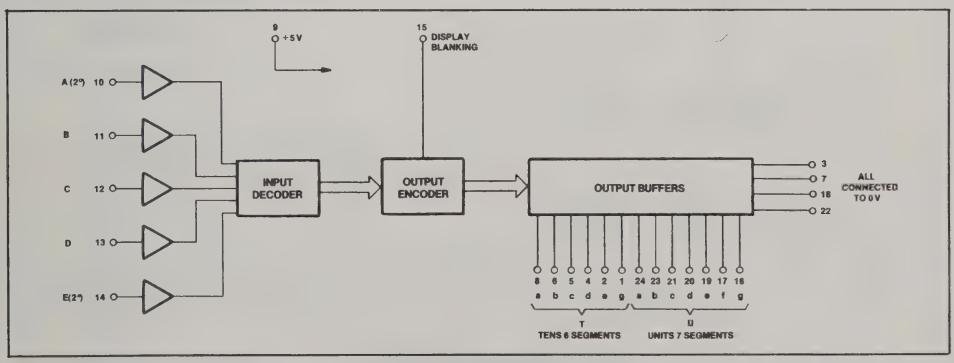

Fig.4 Block diagram

ELECTRICAL CHARACTERISTICS (see Fig.5)

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{DD} = +5V$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	9	4.5	5	5.5	V	
Supply current	9			5	mA	
Input voltage high	10-14	4			V	
Input voltage low	10-14			0.8	V	
Leakage current	10-14			10	μA	$V_{IN} = +5V$
Capacitance	10-14			10	pF	
Output voltage	1, 2, 4-6, 8, 16, 17, 19-21 23, 24			1	V	Sinking 20mA
Recommended series resistor (if used)			120		Ω	

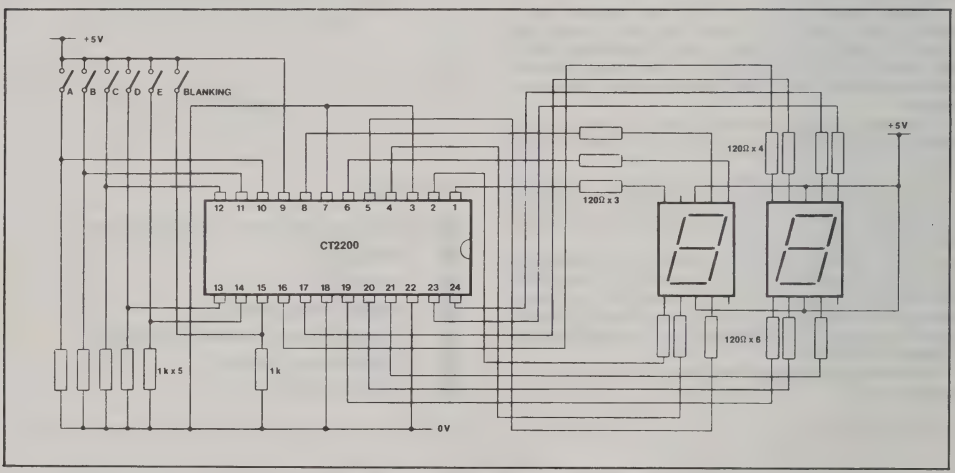

Fig.5 Test circuit and application using load resistors (see also Fig.6)

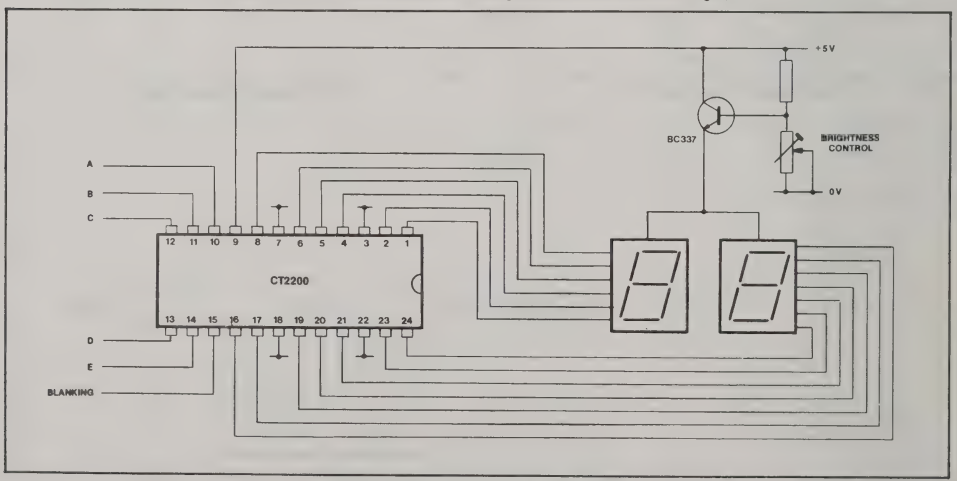

Fig.6 Minimum component application

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	+7V
Input or output voltage	+7V
Output current	30mA
Ambient operating temperature	−10°C to +65°C
Storage temperature	−55°C to +125°C

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ML237B

6-CHANNEL TOUCH CONTROL INTERFACE

The ML237B is a six-channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates - replacing conventional mechanical push-buttons for channel selection. Neons can be used to indicate the selected channel, while the latched output of the ML237B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel output to advance by one.

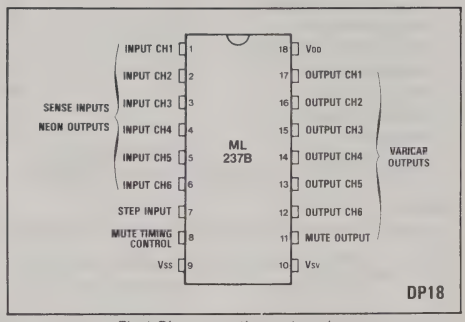


Fig.1 Pin connections - top view

FEATURES

- 6-Channel Capability
- Direct Neon Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selected Channel 1 on Power-up
- Channels Are Selected With a Negative (or Earth) Input

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	-10° C to +65° C
Storage temperature	-10° C to +85° C
Supply, V_{SS}-V_{DD}	36V
Varicap voltage V_{SV}	V_{SS} +0.3V

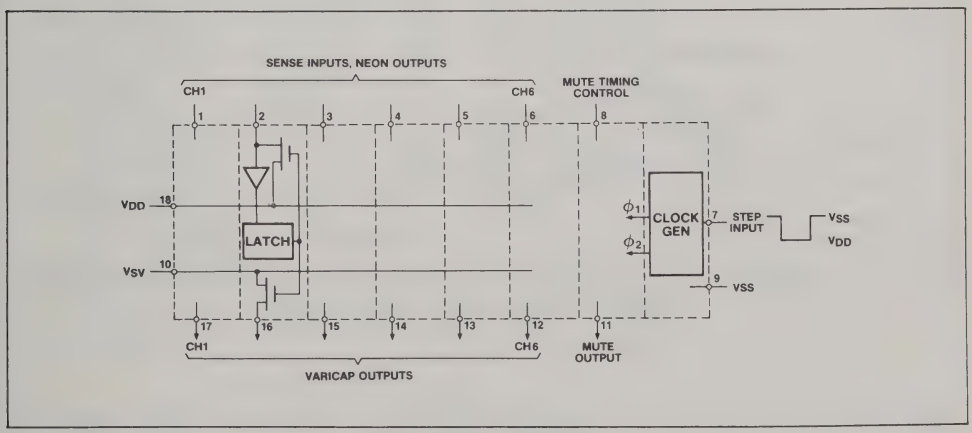


Fig.2 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

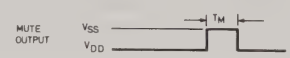
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current			1	μA	$V_{IN} = V_{SS}$
Output leakage			1	μA	V_{OUT} = 0
Mute switch O/P leakage			10	μA	V_{OUT} = 0
Supply current		5	8	mA	
R_{ON} of varicap switch		50	100	Ω	I_{OUT} = 10mA
Step pulse width	0.2			ms	>.05Tm
Neon switch output current			2	mA	
Mute switch R_{ON}		100	200	Ω	I_{OUT} = 5mA
Input threshold	0.4	0.5	0.6	V_{SS}	
Step input current	10		1000	μA	V_{IN} = 0
Mute period		400		ms	C_M = 0.68 μF
Step pulse level	0		V_{SS} −29	V	

NOTES

The mute timing can be increased by using a higher value of capacitor (C_M)

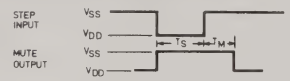
Touch plate selection:



$Tm \simeq Cm \times 0.6ms/nF$

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_S

Stepping selection:



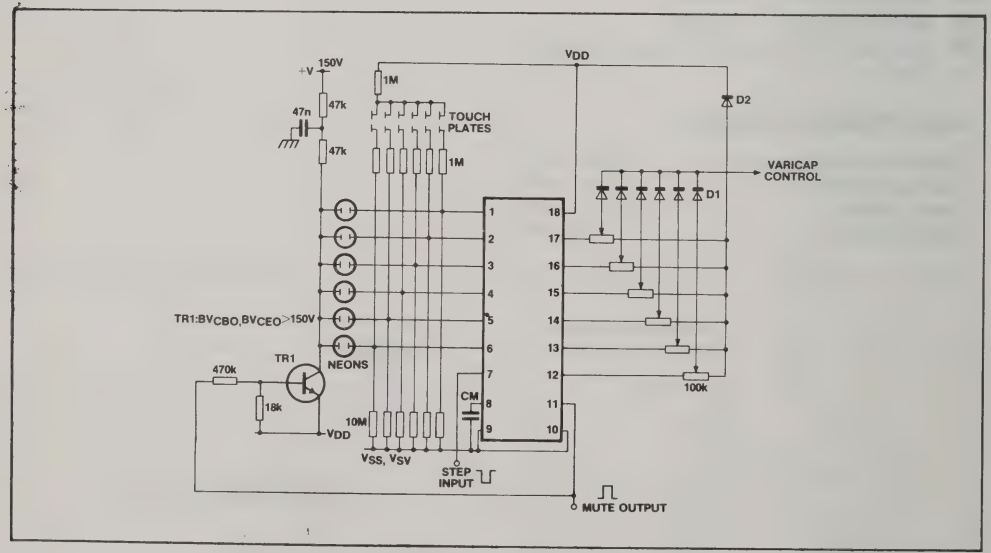


Fig. 3 Typical applications using neons as channel indicators

PLESSEY
Semiconductors

ML238B

8-CHANNEL TOUCH CONTROL INTERFACE

The ML238B is an eight channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates - replacing conventional mechanical push-buttons for channel selection. Neons or LEDs may be used to indicate the selected channel, while the latched output of the ML238B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel to advance by one.

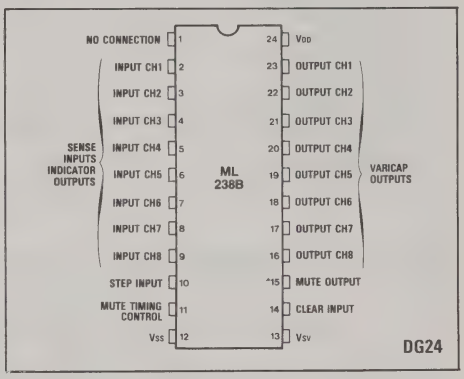


Fig.1 Pin connections - top view

FEATURES

- 8-Channel Capability
- Direct Neon Drive
- Direct Neon or LED Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selects Channel 1 on Power-up
- A Negative Pulse on Clear Resets to Channel 1

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	-10° C to +65° C
Storage temperature	-10° C to +85° C
Supply, V_{SS}-V_{DD}	36V
Varicap voltage V_{SV}	V_{SS} +0.3V

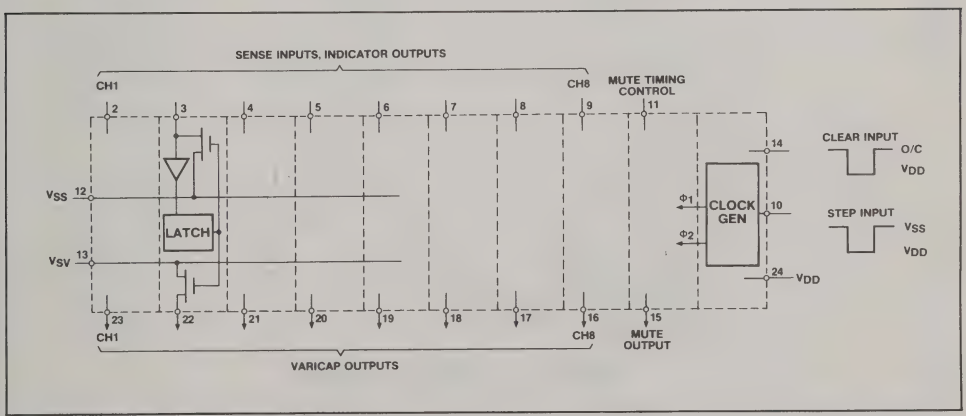


Fig.2 Functional block diagram

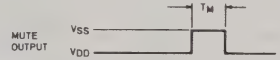
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Output leakage			1	µA	V_{out} = 0
Supply current		6	9	mA	
Input current			1	µA	V_{in} = 0V
R_{ON} of varicap switch		50	100	Ω	I_{OUT} = 10mA
R_{ON} of indicator switch		180	300	Ω	I_{OUT} = 10mA
I/P threshold	0.4	0.5	0.6	V_{SS}	
Step pulse level	0		V_{SS} −29	V	
T_S step pulse width	0.2			ms	>.0 5 Tm
Clear pulse level	0		V_{SS} −29	V	
Clear pulse width	0.2			ms	
R_{ON} of mute switch		100	200	Ω	I_{OUT} = 5mA
T_m mute timing		400		ms	Cm = 0.68µF
Step I/P current	10		1000	µA	V_{in} = 0
Mute O/P leakage			10	µA	V_{OUT} = 0

NOTES:
The mute timing can be increased by using a higher value of capacitor (C_m) (See Fig. 4).

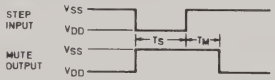
Touch plate selection:



$T_m \simeq C_m \times 0.6ms/nF$

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_s.

Stepping selection:



The clear I/P should be left open circuit when not in use.

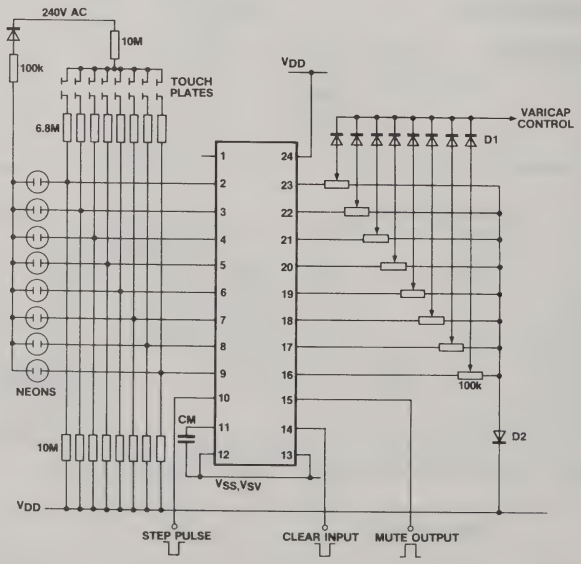


Fig. 3 Typical applications using neons as channel indications

APPLICATION NOTES

Application using LEDs as channel indicators

In applications where the use of mains is not desired channel selection can be made by using the +30V V_{SS} supply as a compromise but at the expense of reduced input sensitivity. In this case LEDs can be used as channel indicators.

The 1.2kΩ and 820Ω resistors limit the LED current to 10mA, whilst the diode ensures less than 1μA leakage when the LED is reverse biased. It is desirable to have a 1MΩ resistor between the touch plates and the input as a safeguard against static.

On selection of a channel, the potential divider chain comprising the 1MΩ resistor, the finger resistance and the 10MΩ resistor sets the threshold voltage on the input pin. When the channel is selected the IC provides a current source to the LED.

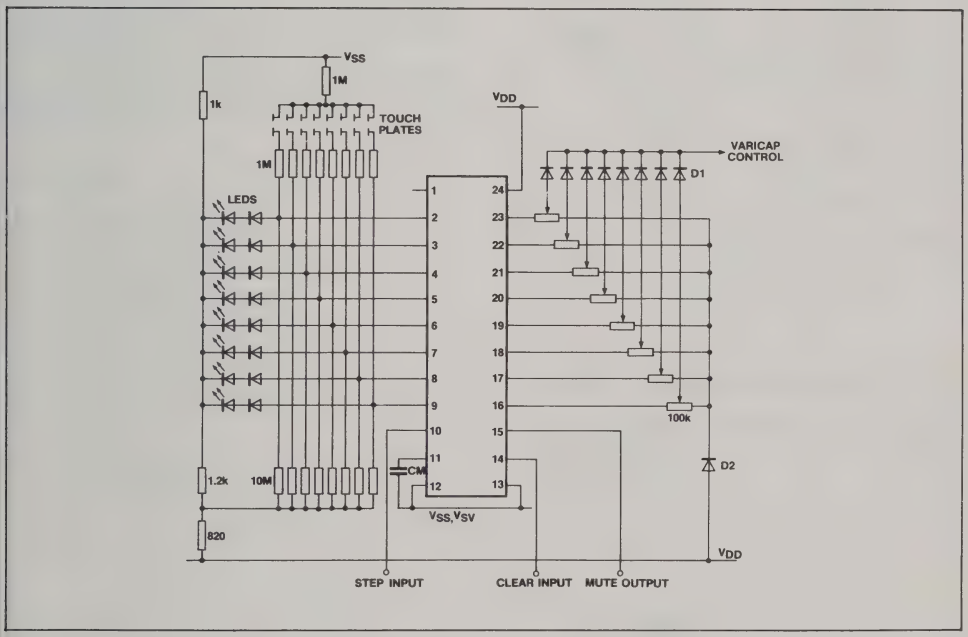


Fig. 4 Low voltage, improved sensitivity using LED indicators

PLESSEY
Semiconductors

ML239B

8 – CHANNEL TOUCH CONTROL INTERFACE

The ML239B is an eight channel sense circuit designed specifically for touch tuning in colour and monochrome television receivers. Using low threshold P-MOS technology, the circuit can be driven directly from two-terminal touch plates – replacing conventional mechanical push-buttons for channel selection. Neons can be used to indicate the selected channel, while the latched output of the ML239B drives the varicap tuner via a bias selection network.

A stepping facility is included whereby the application of a suitable negative-going pulse to the step input causes the selected channel output to advance by one.

FEATURES

- 8-Channel Capability
- Direct Neon Drive
- Low Impedance Drive to Varicap
- Uses 33V Varicap Supply
- Remote Control Stepping Facility
- Sound Muting During Selection
- Selects Channel 1 on Power-up
- A Negative Pulse on Clear Resets to Channel 1
- Channels are Selected with a Negative (or Earth) Input

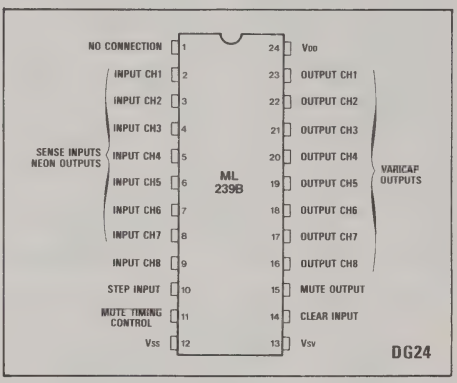


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	–10°C to +65°C
Storage temperature	–10°C to +85°C
V_{SS}–V_{DD} supply	36V
Varicap voltage V_{SV}	V_{SS} +0.3V

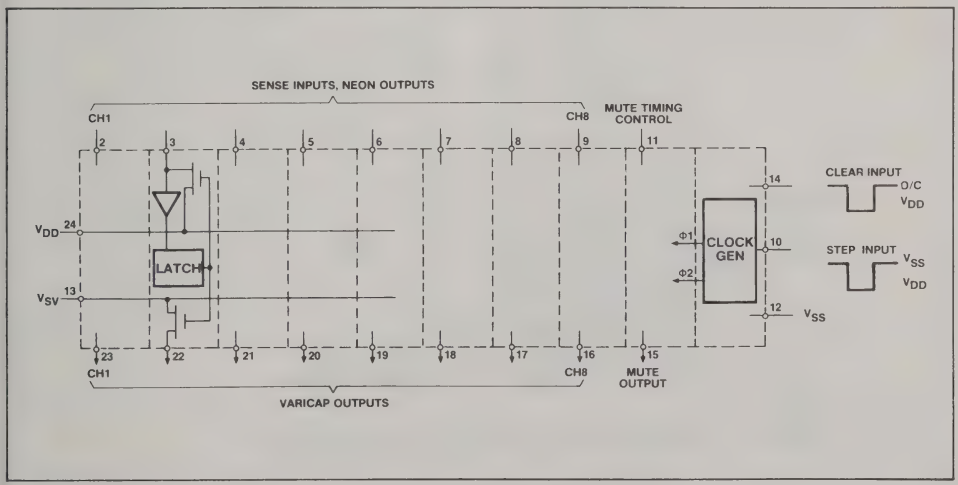


Fig.2 Functional block diagram

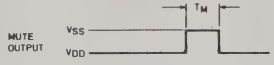
ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 0, V_{SS} = V_{SV} = 30V to 36V

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Step, clear pulse level	0		V_{SS} −29	V	
Input current			1	µA	V_{IN} = V_{SS}
Output leakage			1	µA	V_{OUT} = 0
Mute switch O/P leakage			10	µA	V_{OUT} = 0
Supply current		6	9	mA	
R_{ON} of varicap switch		50	1000	Ω	I_{OUT} = 10mA
Clear step pulse width	0.2			ms	>.05Tm
Neon switch output current			2	mA	
R_{ON} of mute switch		100	200	Ω	I_{OUT} = 5mA
Input threshold	0.4	0.5	0.6	V_{SS}	
Step input current	10		1	mA	V_{IN} = 0
Mute period		400		ms	C_M = 0.68µF

NOTES:
The mute timing can be increased by using a higher value of capacitor (C_m)

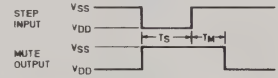
Touch plate selection:



$T_m \simeq C_m \times 0.6ms/nF$

If the channels are selecting by stepping then the mute output is extended by the clock pulse width T_s.

Stepping selection:



The clear I/P should be left open circuit when not in use.

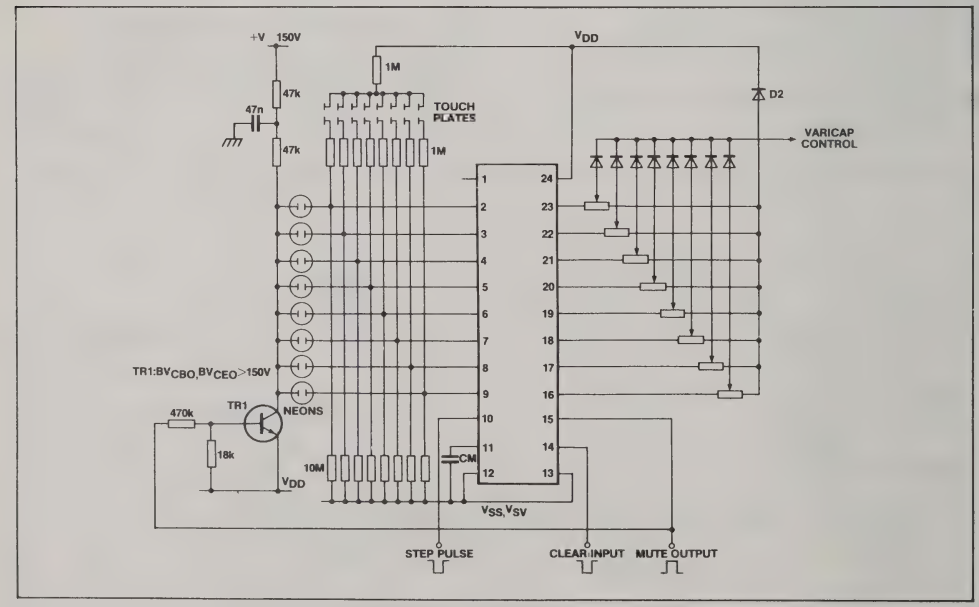


Fig. 3 Typical applications using neons as channel indications

PLESSEY
Semiconductors

ML920

REMOTE CONTROL RECEIVER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML920 decodes the PPM signal received from the SL490 transmitter. After error checking the received code may condition a 20 programme memory or one of three D/A converters.

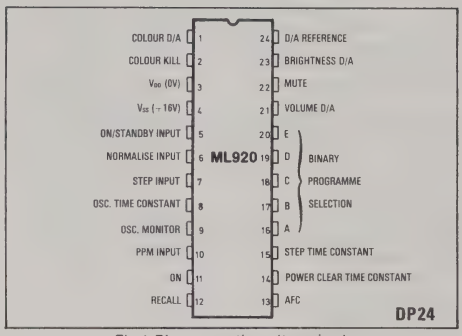


Fig.1 Pin connections (top view)

QUICK REFERENCE DATA

- Power supply: 16V 14mA
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 bit with successive codeword comparison
- Programme: Latched 5 bit binary, 20 programmes
- Analogue controls: 3 static current mirror converters, 32 step with normalise level
- Other outputs: On, Recall Display, AFC, Mute, Colour Kill, Oscillator Monitor
- Local inputs: On/Standby, Step, Normalise

FEATURES

- Accepts 5 Bit PPM
- All Timing From On-Chip Oscillator
- Incorporates Error Protection
- Easily Used with Ultrasonic or Infra-Red System
- Up to 20 Programmes with Latched Binary Output
- 3 D/A Outputs with Normalise Level at ⅜ of Max.
- Automatic Power-On Reset and Normalise
- Many Other Facilities, AFC, Mute, Colour Kill, Recall etc.

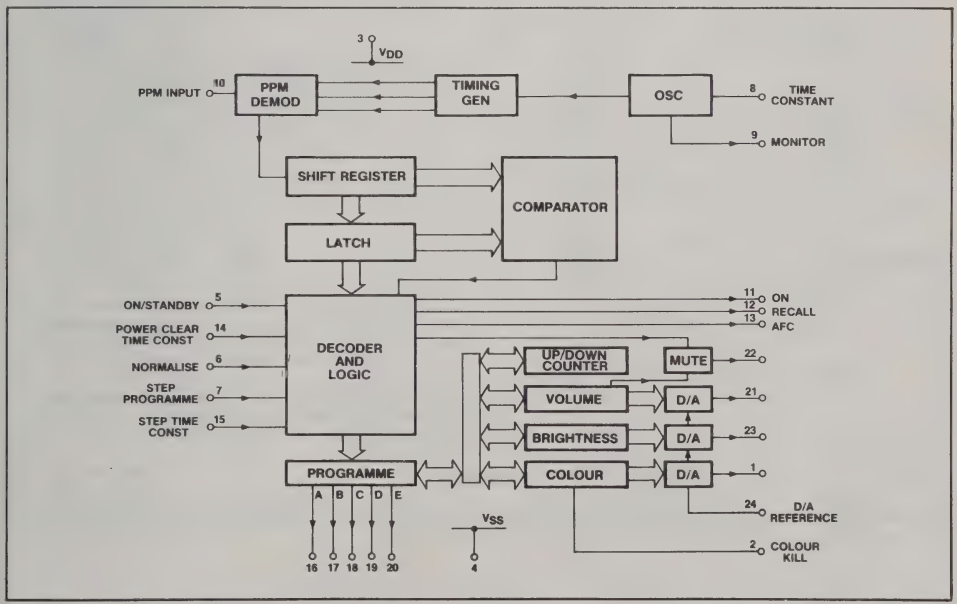


Fig. 2 ML920 remote control receiver block diagram

ELECTRICAL CHARACTERISTICS (see Fig. 3)

Test conditions (unless otherwise stated):

V_{SS} = 0V
V_{DD} = −16V
T_{amb} = 25°C

Characteristics	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	3	14		18	V	
Supply current	3		8	14	mA	
Input logic level high	5, 6, 7,	−1		0	V	
low		V_{DD}		$V_{DD}+3.5$	V	
Output logic level high	2, 11-13, 16-20, 22	−1		0	V	50k to V_{DD}
low		V_{DD}		$V_{DD}+0.5$	V	50k to V_{DD}
Analogue output current range (pins 1, 21, 23)	1, 21, 23	0		$\frac{31}{8}$	I_{REF}	3.9k to V_{DD}
Analogue step size	1, 21, 23	0	$\frac{1}{8}$	$\frac{1}{4}$	I_{REF}	$V_{out} < V_{DD} + 5V$
D/A reference, I_{REF}	24	−250	−345	−455	μA	33k to V_{DD}
Oscillator timing	9		1.5k		Hz	C = 22n, R=100k See note 1
Power clear time constant	14		400		ms	C = 4.7μ R=100k
Step time constant	15		1		s	C = 470n R = 3.3M
Monitor output 'high'	9	−1		0	V	Internal load
'low'		V_{DD}		$V_{DD}+0.5$	V	provided
PPM input level high		−1		0	V	
PPM input level low	10	V_{DD}		−6	V	
PPM input pulse width		1		$22T_{osc}$	μs	$T = \frac{1}{f_{osc}}$

Note 1. Rosc (Pin 8) is 56k-156kΩ, 2fmon (Pin 9) = $f_{osc} \simeq \frac{1}{0.15CR}$ ±20%

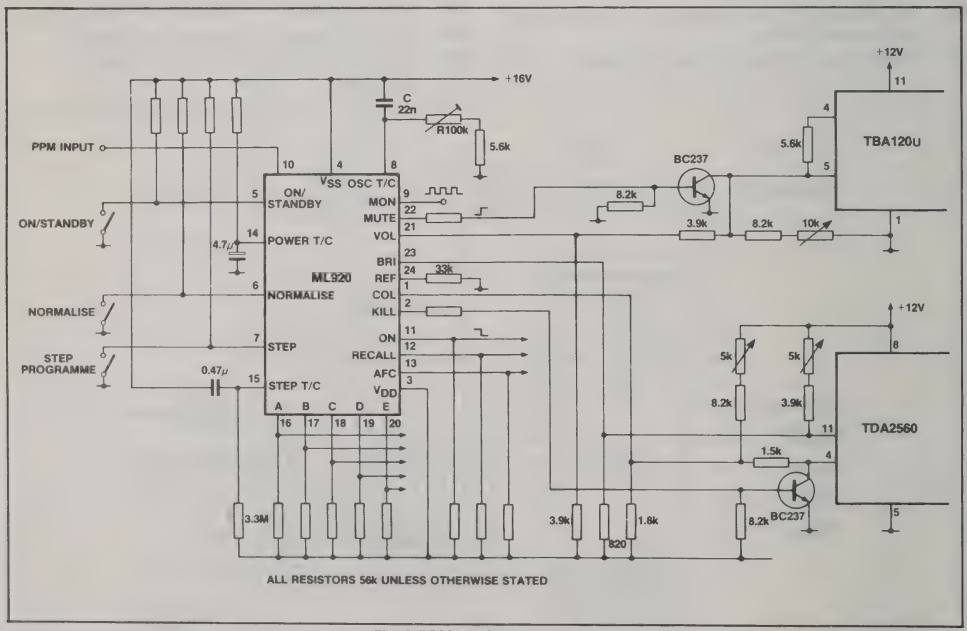


Fig. 3 PPM receiver application

PIN FUNCTIONS

Negative Logic: 0 is 0V (V_{SS}), 1 is −17V (V_{DD})

1, 21, 23. Colour, Volume, Brightness
These three outputs are from three 5 bit current mirror D/A converters. They are referenced to the current drawn from pin 24, I_{ref}, and give 32 steps, $I_{ref}/8$ per step, from 0 to 31/8 I_{ref}. The outputs will be set to 12/8 I_{ref} by the NORMALISE input, the normalise code from the transmitter, or when the ON output goes to a 1.

2. Colour kill
This output gives a logic 0 when the COLOUR D/A output is zero.

3. V_{DD}
−17V power supply

4. V_{SS}
0V power supply

5. On/Standby input
A 1 on this pin will toggle pin 11 (ON O/P), generate RECALL and AFC, normalise VOLUME, BRIGHTNESS and COLOUR, reset MUTE and set channel code 00000.

6. Normalise input
A 1 will normalise the VOLUME, BRIGHTNESS and COLOUR outputs. A RECALL signal is generated and MUTE is reset.

7. Channel step
The channel code will step up by 1 as long as this pin is held at logic 1. The time period between steps is defined by an RC constant attached to pin 15. On reaching 20 the next step returns to 1. On output is set to ON, and AFC is generated. If the TV goes from Standby to ON, RECALL is generated and VOLUME, BRIGHTNESS and COLOUR are normalised. If VOLUME is not 0, MUTE is reset.

8. Oscillator time constant
An RC time constant is formed for the clock timing by connecting external components, one resistor and one capacitor, to this pin. Adjusted so that period of output on pin 9 is 1/20 of 0 interval of incoming PPM.

9. Oscillator monitor
This output is a division of two of the oscillator, and and is available for testing and setting purpose.

10. PPM I/P
The output of the front end amplifier is connected here such that the signal is in the form of positive pulses separated by time periods whose length define the data. With no signal, PPM input is at a low level.

11. On O/P
Open drain output. Logic 1 denotes TV set ON: Logic 0 TV set standby. Set to 1 when channel number changes. Set to 0 by power clear or by transmitter selected Standby. Toggle to opposite state by manual ON/STANDBY control.

12. Recall O/P
Open drain output. A 1 may be used to trigger an on-screen display. A static output is generated by the manual controls ON/STANDBY and NORMALISE.
A pulse is generated by any channel change if the circuit switches to ON at the time, and by RECALL and NORMALISE commands from the transmitter.

13. AFC O/P
Open drain output. Logic 1 can inhibit the tuner AFC.
A static output is generated bymanual ON/STANDBY control. A pulse is generated by any channel number change.

14. Power clear
A capacitor and resistor connected here define the time delay for the power clear circuit, which normalises all D–A outputs etc.

15. Channel step time constant
An R–C time constant defines the time period between increments of the channel number when stepping.

16 –20. Channel outputs
5 Outputs encode 20 channel numbers in binary code

EDCBA
Channel 1 is 00000
Channel 20 is 10011

E is first and A is last in the PPM pulse train.
Channel 1 is set when ON goes to a 1

21. Volume.
See Pin 1

22. Mute O/P
This will change state (toggle) on reception of a mute command and VOLUME O/P is zero MUTE O/P is held at 0.

23. Brightness
See Pin 1

24. D/A Reference
A current drain I_{ref}, set by a single external resistor will set the nominal step of the D/A outputs to $I_{ref}/8$.

Transmitter code	Function
EDCBA	
00000	Programme 1
00001	Programme 2
00010	Programme 3
00011	Programme 4
00100	Programme 5
00101	Programme 6
00110	Programme 7
00111	Programme 8
01000	Programme 9
01001	Programme 10
01010	Programme 11
01011	Programme 12
01100	Programme 13
01101	Programme 14
01110	Programme 15
01111	Programme 16
10000	Programme 17
10001	Programme 18
10010	Programme 19
10011	Programme 20
10100	Colour +
10101	Programme Step +
10110	Volume +
10111	Brightness +
11000	Standby
11001	Mute
11010	Recall
11011	Normalise
11100	Colour −
11101	Programme Step −
11110	Volume −
11111	Brightness −

Table 1 Basic 32 command set

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V).

Supply Voltage V_{DD}	+0.3V to −25V
Voltage at any input	+0.3V to −25V
Operating voltage range, V_{DD}	−14V to −18V
Maximum power dissipation	600mW
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

PLESSEY
Semiconductors

ML922

REMOTE CONTROL RECEIVER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML922 decodes the PPM signal received from the SL490 transmitter. After error checking the received code may condition a 10 programme memory or one of three D/A converters.

The receiver timing may be set by adjusting the oscillator time constant to give 40 periods at pin 6 equal to a 0 interval on the received PPM input.

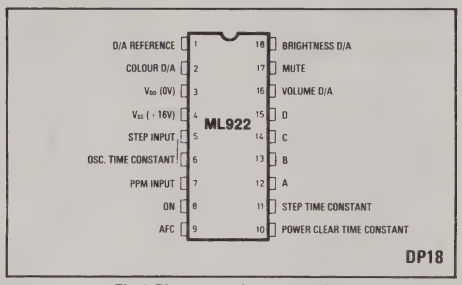


Fig.1 Pin connections - top view

FEATURES

- Accepts 5 Bit PPM
- All Timing From On-Chip Oscillator
- Incorporates Error Protection
- Easily Used With Ultrasonic or Infra-red System
- Up to 10 Programmes With Latched Binary Output
- 3 D/A Outputs With Normalise Level At $\frac{3}{8}$ of Max.
- Automatic Power-On Reset and Normalise
- Many Other Facilities, AFC, Mute, Etc.

QUICK REFERENCE DATA

- Power supply: 16V 14mA
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 bit with successive codeword comparison
- Programme: Latched 4 bit binary, 10 programmes
- Other outputs: On, AFC, Mute
- Local inputs: Programme step

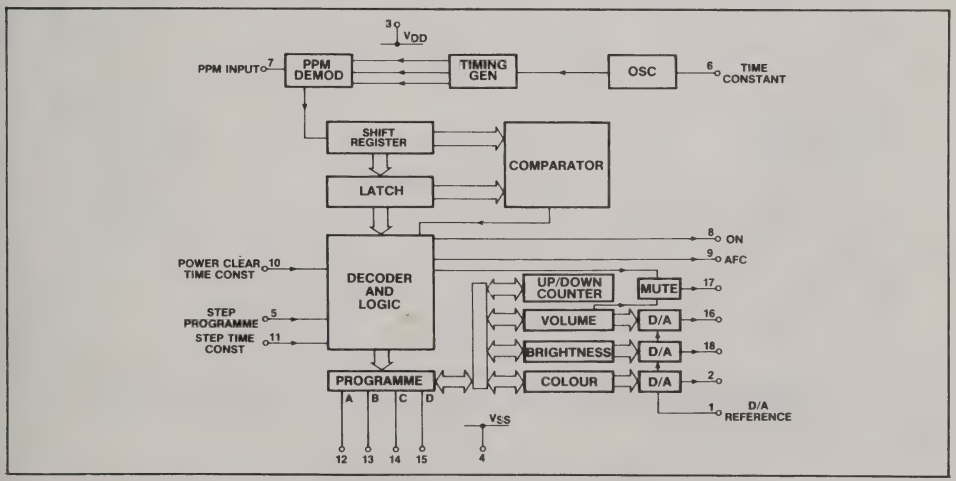


Fig. 2 ML922 remote control receiver block diagram

ELECTRICAL CHARACTERISTICS (see Fig. 3)

Test conditions (unless otherwise stated):

$V_{SS} = 0V$
$V_{DD} = -16V$
$T_{amb} = 25°C$

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	3	14		18	V	
Supply current	3		8	14	mA	
Input logic level high	5	−1		0	V	
low		V_{DD}		$V_{DD} + 3.5$	V	
Output logic level high	8, 9, 12-15, 17	−1		0	V	50k to V_{DD}
low		V_{DD}		$V_{DD} + 0.5$	V	50k to V_{DD}
Analogue output current range	2, 16, 18	0		$\frac{31}{8}$	I_{ref}	3.9k to V_{DD}
Analogue step size	2, 16, 18	0	$\frac{1}{8}$	$\frac{1}{4}$	I_{ref}	$V_{out} < V_{DD} + 5V$
D/A reference, I_{REF}	1	−250	−345	−455	μA	33k to V_{DD}
Oscillator timing	6		3		kHz	C = 22n, R = 100k See note 1
Power clear time constant	10		400		ms	C = 4.7μ R = 100k
Step time constant	11		2		s	C = 470n R = 3.3M
PPM input level high	7	-1		0	V	
PPM input level low	7	V_{DD}		-6	V	
PPM input pulse width	7	1		$22T_{OSC}$	μs	

Note 1. $R_{osc.}$ (pin 6) is 56k-156kΩ. $f_{osc.} \simeq \frac{1}{0.15CR^{1}} \pm 20\%$

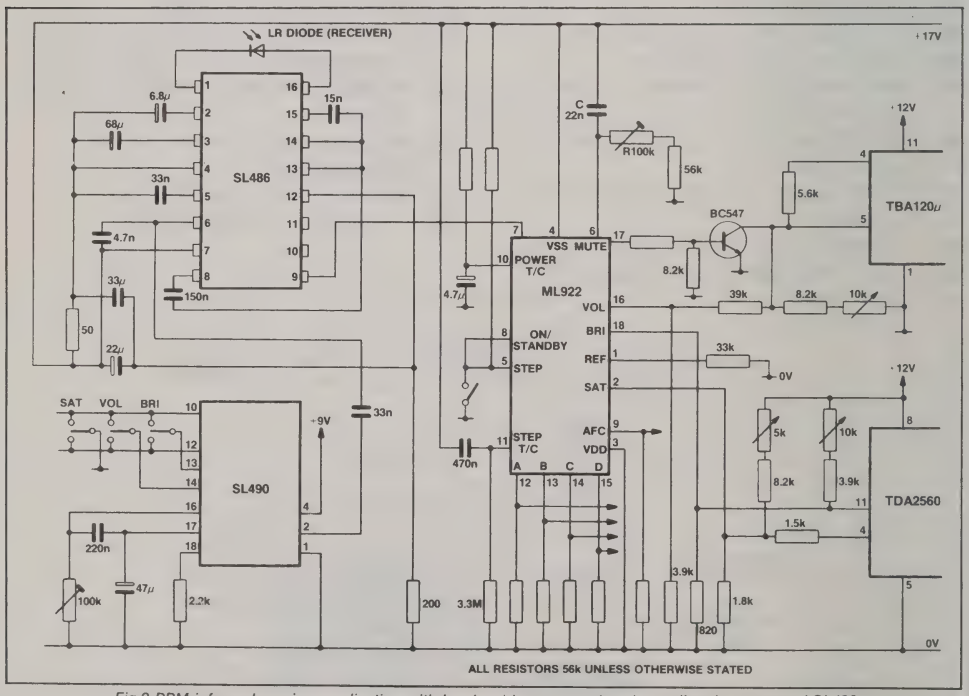


Fig.3 PPM infra-red receiver application with local up/down controls using a directly connected SL490

Note: Pin descriptions same as ML920.

Transmitter code	Function
EDCBA	
0000X	Programme 1
0001X	Programme 2
0010X	Programme 3
0011X	Programme 4
0100X	Programme 5
0101X	Programme 6
0110X	Programme 7
0111X	Programme 8
1000X	Programme 9
1001X	Programme 10
10100	Colour +
10101	Programme Step +
10110	Volume +
10111	Brightness +
11000	Standby
11001	Mute (Analogue 2)
11011	Normalise
11100	Colour —
11101	Programme Step —
11110	Volume —
11111	Brightness —

Table 1 Basic 21 command set for ML922

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V).

Supply Voltage V_{DD}	+0.3V to −25V
Voltage at any input	+0.3V to −25V
Maximum power dissipation	600mW
Operating temperature range	−10°C to +65°C
Storage temperature range	−55°C to +125°C

PLESSEY
Semiconductors

ML923

REMOTE CONTROL RECEIVER

The ML923 is an MOS/LSI monolithic integrated circuit for use as a receiver of remote control signals for television control. It accepts 24 of the 32 codes transmitted by the SL490 transmitter circuit in the Pulse Position Modulation (PPM) method of coding.

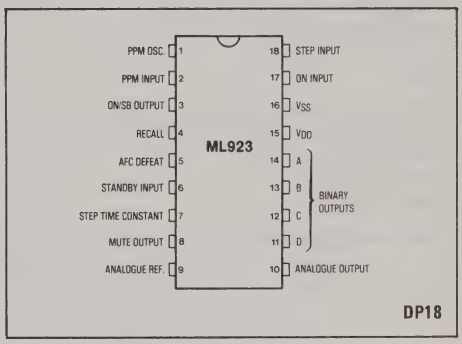


Fig.1 Pin connections top view

FEATURES

- 16 Channel Selection Codes
- Single Analogue Output
- Mute Output (Toggle)
- On-set Controls—Channel Step, ON, Reset
- Normalise to $\frac{3}{8}$ of Max Output on Analogue Output
- Outputs Provide Control of ON/STANDBY, Analogue Mute, and AFC Defeat
- Choice of Power-Up Function:
  a) Power Up to Standby State, Switch to ON State by Local or Remote Command and STANDBY by Remote Command.
  b) Power Up to ON State, Switch OFF with Solenoid Operated Mains Switch by Local or Remote Command.

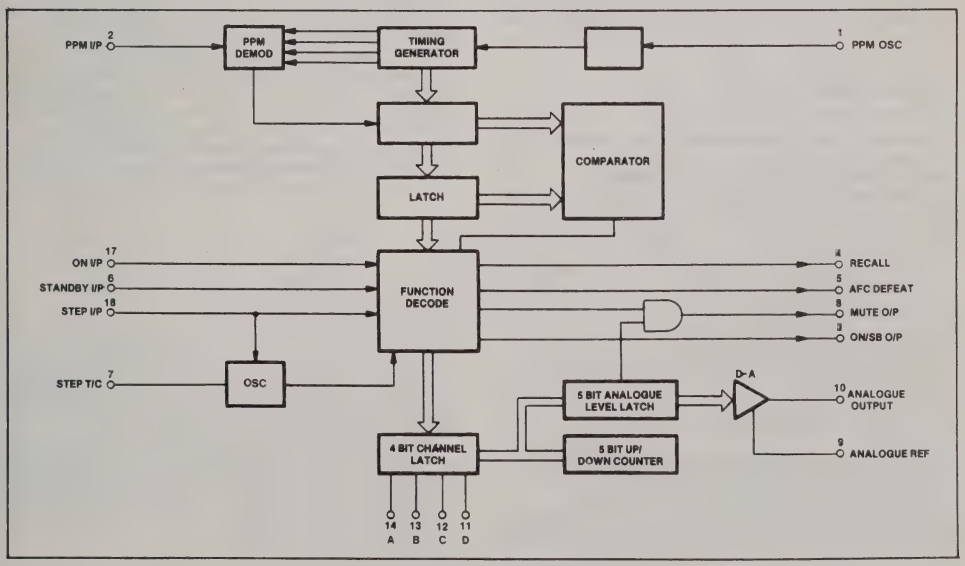


Fig.2 ML923 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $V_{SS} = 0V$, $V_{DD} = -16V$

Characteristics	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	1	14		18	V	
Supply current	1		6		mA	
Input logic level high	6, 17, 18	-1		0	V	
Input logic level low		V_{DD}		$V_{DD}+3.5$	V	
Output logic level high	3, 4, 11, 14	-1.5		0V	V	50k to V_{DD}
Output logic level low	8	V_{DD}		$V_{DD}+0.5$	V	
Analogue output current range	10	0		$\frac{31}{8}$	1 Ref	3.9k to V_{DD}
Analogue step size	10	0	$\frac{1}{8}$	$\frac{1}{4}$	1 Ref	$V_{out} < V_{DD}+5V$
D/A reference, I ref	9	-250	-345	-455	mA	33kΩ to V_{DD}
PPM		15		150k	Hz	Typical TC
Oscillator frequency	1		3k		Hz	C = 22nF R = 100kΩ
On input or standby input time constant for power on	6 or 17	250		500	ms	
Step time constant	7		1		s	C = 470nF R = 3.3MΩ
PPM input level high	2	-1		0	V	
PPM input level low	2	V_{DD}		-6	V	
PPM input pulse width	2	1		22 T_{osc}	μs	$T = \frac{1}{f_{osc}}$

Note 1 R_{osc} (pin 5) is 56k-156kΩ $f_{osc} \simeq \frac{1}{0.15CR}$ ±20%

OPERATING NOTES

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to different transmission rates within the same operating area).

Checks are made to ensure 6 pulses, or 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code. Channel step time period is derived from an external time constant.

PIN FUNCTIONS

Positive Logic: Logic '1' = V_{SS}, 0V Logic '0' = V_{DD}, -16V

1. Oscillator Time Constant An RC Time Constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

2. PPM Input The output of the Front End Amplifier is connected to the pin; the signal must consist of a normal low level with pulses to high level, corresponding to the PPM pulse from the transmitter.

3. ON/SB Output Open drain output. Logic '0' denotes onset. Logic '1' standby set. Set to '0' when channel number changes, and by ON input at logic '0', set to '1' by standby input or by transmitter selected OFF.

4. Recall O/P Open drain output. A '0' may be used to trigger an on-screen display. A '0' is output during an input at pin 17, ON input. The pulse to logic '0' is generated by any channel change if circuit switches to ON from Standby, and by recall and normalise commands from the remote transmitter.

5. AFC O/P Open drain output. A logic '0' can inhibit tuner AFC. A static output is generated by manual ON control. A pulse is generated by any channel number change.

6. Standby Input A logic '0' will select standby state and normalise the analogue output to 3/8 maximum and select programme 1. An RC time constant may be connected to select standby at power ON.

7. Channel Step Time Constant An RC time constant defines the time period between increments of the channel number when stepping.

8. MUTE Output This will change state (toggle) on receptin of a Mute command or will remain at logic '1' if the D-A output is zero. The output is reset by any channel change command.

9. Analogue Reference A current drain attached to this input will define the current step of the D-A output. The current is equal to 8 output current steps.

10. Analogue Output The output of a current mirror D-A convertor provides a current source of between 0mA and 1.3mA. It is variable in 32 steps, UP or DOWN. It is normalised to 3/8 maximum value by the ON/SB input, and by normalise command from the transmitter.

11, 12, 13, 14. Channel Selection Outputs These outputs encode the 16 channels in binary code.

	A	B	C	D
Channel 1	0	0	0	0
Channel 16	1	1	1	1

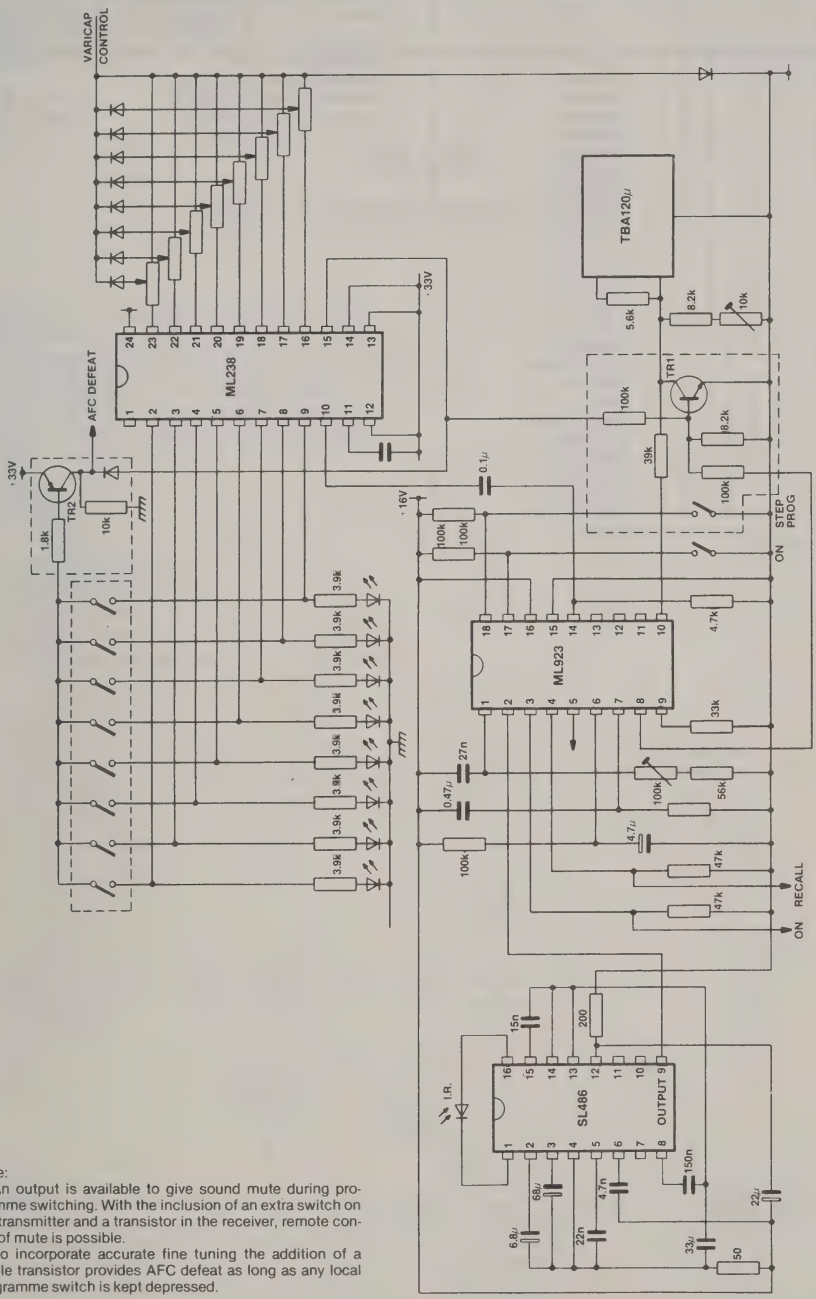
Set to channel 1 on set switch ON.

15. V_{DD} -14V to -18V power supply

16. V_{SS} 0V (Ground)

17. ON I/P A logic '0' will switch the ON/SB output to ON (logic '0'). Channel 1 is selected and analogue output is normalised to 3/8 maximum. An RC time constant may be connected to select set ON at power on. The AFC defeat signal is generated and Mute is reset.

18. Step Input The channel code will step up by 1 as long as the pin is held at logic '0'. The time period between steps is defined by an RC constant on pin 7. When the channel code reaches 16 it will go to 1 next step. A step input will set ON/SB output to ON and normalise the analogue output. Mute is reset if analogue = 0.



Note:
1. An output is available to give sound mute during programme switching. With the inclusion of an extra switch on the transmitter and a transistor in the receiver, remote control of mute is possible.
2. To incorporate accurate fine tuning the addition of a single transistor provides AFC defeat as long as any local programme switch is kept depressed.

Fig.3 Receiver application

CODE					FUNCTION
E	D	C	B	A	
0	0	0	0	0	Channel 1
0	0	0	0	1	Channel 2
0	0	0	1	0	Channel 3
0	0	0	1	1	Channel 4
0	0	1	0	0	Channel 5
0	0	1	0	1	Channel 6
0	0	1	1	0	Channel 7
0	0	1	1	1	Channel 8
0	1	0	0	0	Channel 9
0	1	0	0	1	Channel 10
0	1	0	1	0	Channel 11
0	1	0	1	1	Channel 12
0	1	1	0	0	Channel 13
0	1	1	0	1	Channel 14
0	1	1	1	0	Channel 15
0	1	1	1	1	Channel 16
1	0	1	0	1	Channel Step +
1	0	1	0	0	Analogue +
1	1	0	1	0	Recall
1	1	0	0	1	Mute (Toggle)
1	1	0	1	1	Normalise
1	1	0	0	0	OFF
1	1	1	0	1	Channel Step–
1	1	1	0	0	Analogue–

Table 1 Command set

ABSOLUTE MAXIMUM RATINGS (Vss = 0V).

Supply Voltage V_{DD}	+0.3V to -25V
Voltage at any input	+0.3V to -25V
Maximum power dissipation	600mW
Operating temperature range	-10° C to +65° C
Storage temperature range	-55° C to +125° C

PLESSEY
Semiconductors

ML924

REMOTE CONTROL RECEIVER

The ML924 is an MOS/LSI integrated circuit for use as a receiver of remote control signals generated by the SL490 transmitter circuit, using PPM (Pulse Position Modulation) encoding technique. The receiver has 5 digital outputs whose response to PPM codes may be programmed by six control lines. It has a handshake interface which provides communication with microprocessors and computers.

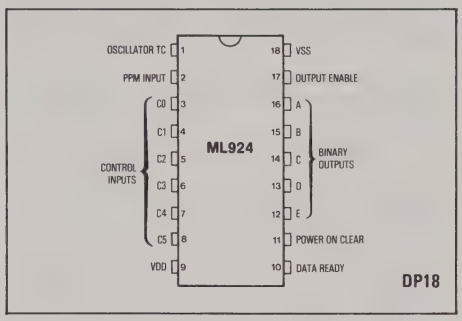


Fig.1 Pin connections top view

FEATURES

- 5 Open Drain Outputs with Enable
- Handshake or Interrupt Microprocessor and Computer Interface Signals
- On-Chip Oscillator
- 6 Control Lines to Programme Output Response
- 3 Selectable Output Modes

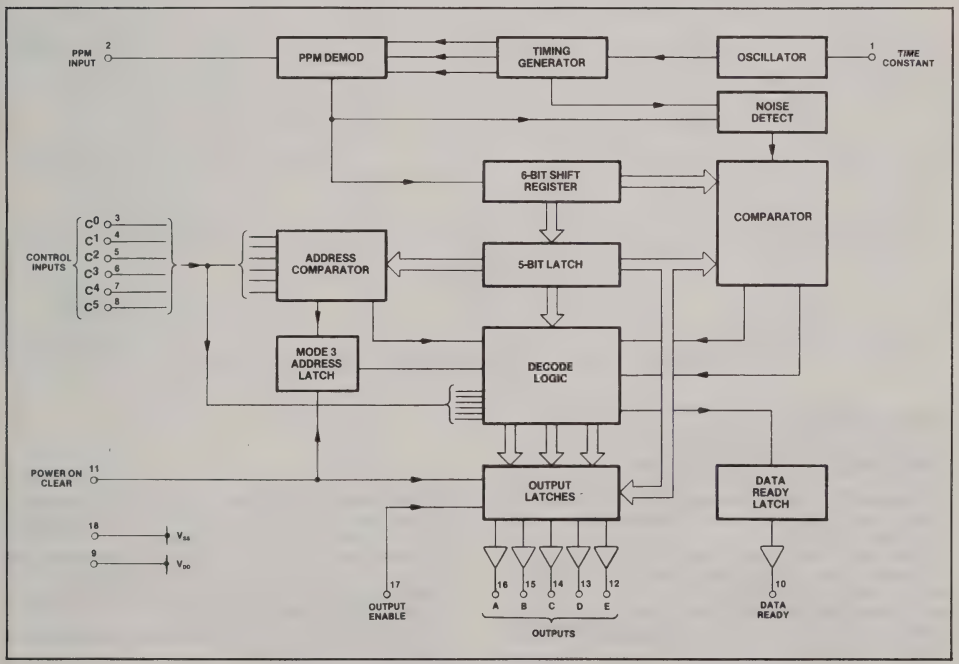


Fig.2 ML924 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{SS} = 0V$; $V_{DD} = -16V$; $T_{amb} = +25°C$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	9	12		18	V	
Supply current	9		6		mA	
Input logic level high ('1')	3-8,17	-1		0	V	
Input logic level low ('0')		V_{DD}		$V_{DD} + 3.5$	V	
Output logic level high ('1')	10,12-16	-1		0V		50k to V_{DD}
Output logic level low ('0')		V_{DD}		$V_{DD} + 0.5$	V	
Oscillator frequency	1	15	3k	150k	Hz	Typical TC: C = 22nF, R = 100kΩ
PPM input level high	2	-1		0V		
PPM input level low		V_{DD}		-6V		
PPM input pulse width	2	1		$22T_{osc}$	μs	$T = \frac{1}{f_{osc}}$
Power clear time constant	11	1	400		ms	

NOTE

Rosc (Pin 1) is 56kΩ to 156kΩ, $fosc \simeq \frac{1}{0.15\,CR}$ ±20%

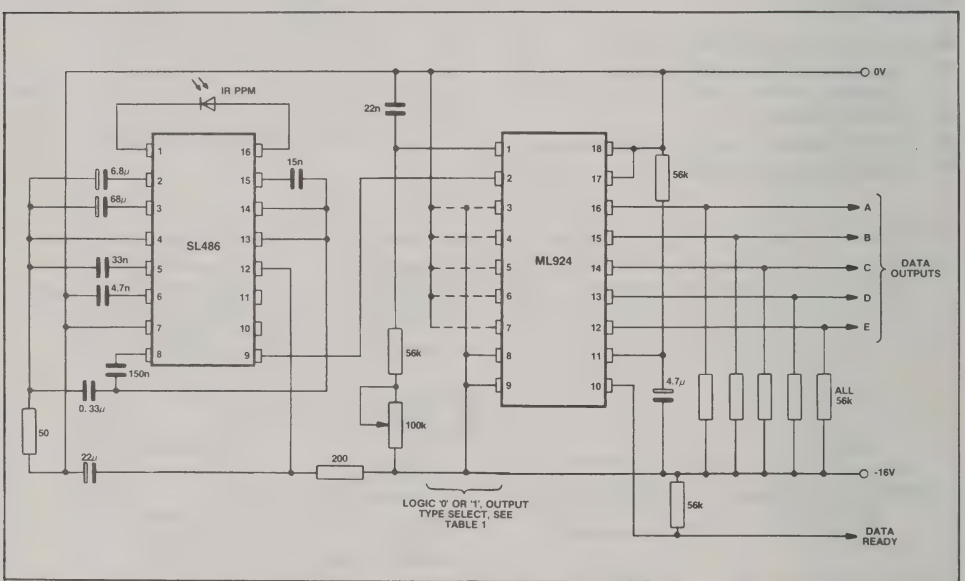


Fig.3 Application for receiving 32 codes, from SL490 transmitter, in mode 1

PIN FUNCTIONS

Positive Logic: Logic '1' = V_{SS}, 0V Logic '0' = V_{DD}, -16V

1. Oscillator TC An RC time constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.
2. PPM Input The output of the Front End Amplifier is connected to this pin; the signal must consist of a normal low level with pulses to the high state.
3-8. Control Word C_0 to C_5 Six control bits form the control word which programs the response of the five outputs (see Table 1).
9. V_{DD} -12V to -18V power supply.
10. Data Ready Open drain output. An output of logic '1' indicates the reception of a valid PPM word. It will remain at logic '1' for the duration of transmission.
11. Power Clear A capacitor and resistor connected to this pin define the time delay for the Power Clear Circuit.
12-16. Outputs E-A Open drain outputs which respond to the PPM input as defined in Table 1.
17. Output Enable A logic '1' will enable outputs A to E. A logic '0' will turn all outputs off.
18. V_{SS} 0V (Ground).

APPLICATION NOTES

By setting combinations of logic states on the six control line inputs, C_0 to C_5 (pins 3 to 8), the outputs E to A (pins 12 to 16) on the ML924, can respond to the PPM input word (as shown in Fig.4) in three modes, detailed below:

Control Mode 1

Each output E to A directly corresponds to bits e to a in the PPM word. The type of output available can be either latched (LA) or momentary (M) according to the combination of C_0 to C_5 used, as given in Table 1. This mode allows direct control of all five bits on one receiver, by the 32 codes from an SL490 transmitter. Fig.3 shows the ML924 used in this mode in conjunction with an SL486 infra-red pre-amplifier.

Control Mode 2

Bits a and b, in the PPM input word, address one of up to four (binary 0 to 3) receivers that has been correspondingly designated that number (W_1W_0), by bits C_0 and C_1 in the control word (Table 1). Bits c and d in the PPM input word, address one of four outputs D to A, on this addressed receiver (Table 1, note 2), via code V_1V_0. Output E is not used.

Bits C_2 to C_5, in the control word, select combinations of output types; either set/reset (S/R) or momentary (M) as shown in Table 1. The addressed output (V_1V_0) on the addressed receiver (W_1W_0) will either be reset by bit e of the PPM input word (logic '0'), or set (pulsed if momentary type output), if bit e is logic '1'.

This mode thus allows the state of up to 16 bits (4 each on 4 receivers), to be individually controlled by the PPM input word, with the 32 codes from an SL490 transmitter. Table 2(a) shows, in detail, the received code interpretation for mode 2.

Control Mode 3

The PPM input word can be interpreted as address or data, depending on the logic state of bit e. If bit e is logic '0', bits a to d address one of up to sixteen (binary 0 to 15) receivers that has been correspondingly designated that number ($U_3U_2U_1U_0$) by bits C_0 to C_3 in the control word (Table 1). If bit e is logic '1', then bits a to d correspond to the outputs A to D on the currently addressed receiver.

The output types can either be all latched (LA) or all momentary (M), depending on the logic state of control bits C_4 and C_5 (Table 1).

Output E of the currently addressed receiver is used as an address acknowledge output (true high), and will go high upon reception of a valid address code. This output will remain high until reception of an invalid address code, or a power-on reset. Thus, only one of the sixteen possible bit E outputs will be high at any one time.

In this manner, up to sixty-four bits (four bits each on sixteen receivers) can be individually controlled by the PPM input word, with the 32 codes from an SL490 transmitter. Fig.5 outlines the application diagram for mode 3, using the maximum possible number of receivers (for one PPM rate). Details of the input PPM code interpretation for mode 3 are given in Table 2(b).

In all modes, taking the output enable input (pin 17) low swithces off all the outputs, except data ready, but the device retains the data internally.

The momentary (M) type of output means that data is available during reception of the PPM input word only, i.e. after a valid word has been detected by the ML924. A valid word is realised when two successive identical PPM input words are detected. The DATA READY output is at logic '1' during the reception of a valid PPM input word. All momentary outputs will be returned to zero when reception of the valid PPM input word ceases (i.e. a successive word is different or absent from the preceding word). DATA READY will also return to the zero state. If the latched (LA) type of output has been chosen, the received data will be latched and retained when reception ceases. Note also that in mode 3 a valid (matched) received address code is also latched. Similarly, for a set/reset (S/R) type of output, data is retained when reception ceases.

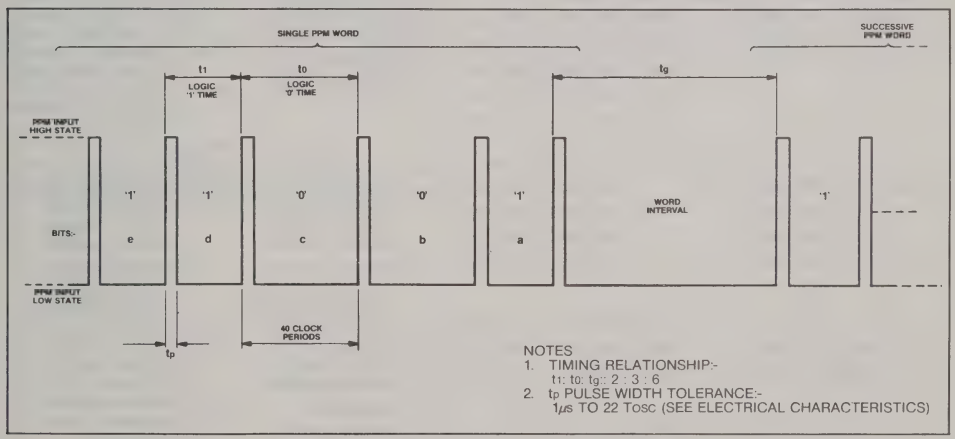
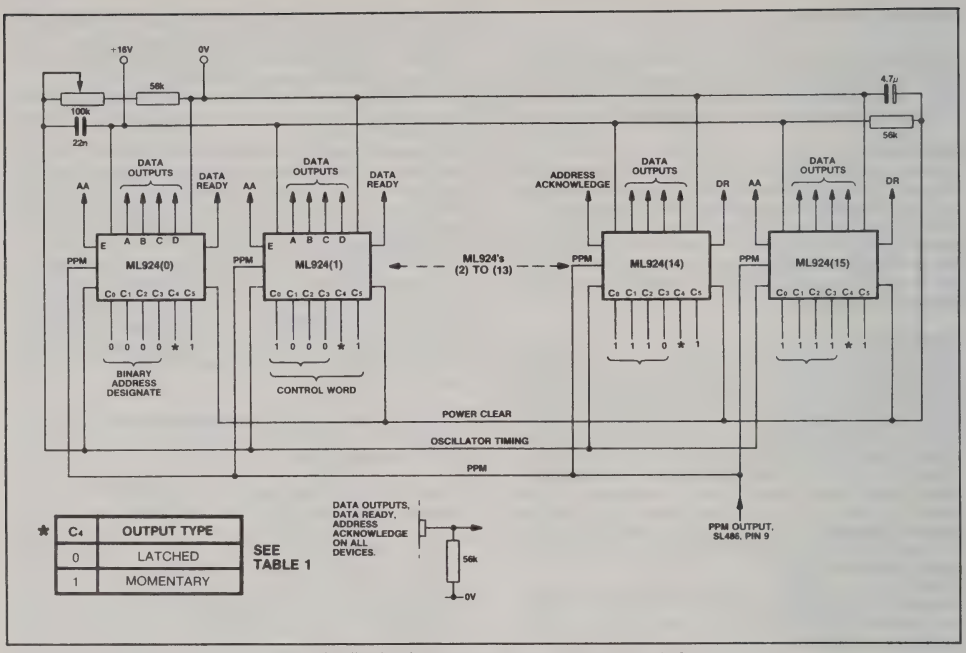


Fig.4 PPM input word format, showing 11001 example



★ C4	OUTPUT TYPE
0	LATCHED
1	MOMENTARY

Fig.5 Application for controlling up to 64 bits in mode 3

Control word						Control mode	Output response					Interpretation of PPM input words	
C5	C4	C3	C2	C1	C0		E	D	C	B	A	e d c b a	e d c b a
0	0	0	0	0	0	1	LA	LA	LA	LA	LA	E D C B A	
0	0	0	0	0	1	1	LA	LA	LA	LA	M	PPM decoded on all outputs directly	
0	0	0	0	1	1	1	LA	LA	LA	M	M		
0	0	0	1	1	1	1	LA	LA	M	M	M		
0	0	1	1	1	1	1	LA	M	M	M	M		
0	1	1	1	1	1	1	M	M	M	M	M		
0	0	1	0	W1	W0	2	-	S/R	S/R	S/R	S/R	0 V1 V0 W1 W0	1 V1 V0 W1 W0
0	1	0	0	W1	W0	2	-	S/R	S/R	S/R	M	Output address / Receiver address	Output address / Receiver address
0	1	0	1	W1	W0	2	-	S/R	S/R	M	M	Resets an S/R type output. No effect on a momentary output.	Sets an S/R type output, or pulses a momentary output.
0	1	1	0	W1	W0	2	-	S/R	M	M	M		
1	0	U3	U2	U1	U0	3	AA	LA	LA	LA	LA	0 U3 U2 U1 U0	1 D C B A
1	1	U3	U2	U1	U0	3	AA	M	M	M	M	Receiver address / Designates address mode	PPM data Sent to outputs on addressed receiver / Designates data mode

Table 1 Interpretation of ML924 control word

NOTES
1. Control mode 1 : Direct response to the PPM code.
2. Control mode 2 : W_1W_0 is a 2 bit address for the receiver, designated W_1W_0 by the control word. V_1V_0 selects one of 4 outputs on the addressed receiver.

V_1	V_0	Addressed output
0	0	A (Pin 16)
0	1	B (Pin 15)
1	0	C (Pin 14)
1	0	D (Pin 13)

3. Control mode 3 : $U_3U_2U_1U_0$ is a 4 bit address that selects, by means of 16 PPM codes, the receiver designated $U_3U_2U_1U_0$ by the control word, when bit e of the PPM code is '0'. If bit e is '1', the 4 outputs A to D on the currently addressed receiver are directly controlled by bits a to d.
4. Control mode 3 : The E output of the receiver acts as an address acknowledge (AA) output. This goes high when a receiver detects a valid address instruction, and indicates that it will receive subsequent data transmission.

OPERATING NOTES

Receiver Oscillator

The receiver operates on a time scale fixed by an internal oscillator and its external components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receiver systems to respond to different transmission rates within the same area). If more than one ML924 is being used in a receiver system (control modes 2 or 3) the oscillators can be connected together, still allowing the receiver system timing to be set with one adjustment only. In other words, only one RC arrangement is needed, with pin 1 on all ML924's connected together for the devices constituting the single receiver system.

Setting Up Procedure

When designing a system using the SL490/491 transmitters and the ML924 receiver, it is not necessary to adjust the PPM rate on both transmitter and receiver. The usual arrangement is to have a fixed resistor of 33k from pin 16 of the SL490/491 and to choose the capacitor connected for pin 16 to pin 17 to give the required PPM rate. The value is calculated from the formula $t_o = 1.4CR$. Provided fairly close tolerance components are used for C1 and R1, then assembled transmitter units should be interchangeable without adjustment.

The timing components on the ML924 receiver can be selected using the formula

$$f_{rx} = \frac{1}{0.15CR} \text{ where } f_{rx} = \frac{40}{t_o}$$

t_o being the PPM logic 0 time from the transmitter.

The value of R for the receiver should be between 47k and 200k, a typical arrangement being to use a 47k fixed resistor and a 100k pot as shown in Fig.6. The capacitor should be selected from the above formula to give the nominal frequency somewhere near the mid-range setting of the potentiometer.

Final adjustment is made by setting the period on the receiver oscillator time constant pin to 1/40th of the transmitter PPM logic '0' time using the potentiometer. Connection to the receiver time constant pin should be made using a x10 oscilloscope probe to reduce circuit loading.

Maximum Bit Control

In all modes, the maximum possible number of bits that can be controlled by one 32 code transmitter, can be increased by using more than one PPM rate. For example, it is possible to control a maximum of 128 bits in mode 3, by using 16 receivers operating on one PPM rate, and 16 receivers operating on a second PPM rate separated from the first by a factor of at least 2. If using an SL490 transmitter, a transmission rate of n and (nx2) may be incorporated in one device application, thus allowing 128 bits t be controlled by one 32 code transmitter.

PPM word bits	a b	a b	a b	a b	W_0W_1	c	d	e
	1 1	0 1	1 0	0 0				
Receiver address/ control word bits	C_0 C_1 1 1	C_0 C_1 0 1	C_0 C_1 1 0	C_0 C_1 0 0				
Sets an S/R type output to 1; pulses momentary output	31	30	29	28	V_0V_1	1 1 D		1
	27	26	25	24	V_0V_1	0 1 C		1
	23	22	21	20	V_0V_1	1 0 B		1
	19	18	17	16	V_0V_1	0 0 A		1
Resets an S/R type output to zero; no change momentary output	15	14	13	12	V_0V_1	1 1 D		0
	11	10	9	8	V_0V_1	0 1 C		0
	7	6	5	4	V_0V_1	1 0 B		0
	3	2	1	0	V_0V_1	0 0 A		0

Decimal equivalent codes (a) mode 2

ML924 output address

PPM word bits	a b	a b	a b	a b	c	d	e
	1 1	0 1	1 0	0 0			
Receiver address/ control word bits	C_0 C_1 1 1	C_0 C_1 0 1	C_0 C_1 1 0	C_0 C_1 0 0	C_2	C_3	
Output data	31	30	29	28	1	1	1
	27	26	25	24	0	1	1
	23	22	21	20	1	0	1
	19	18	17	16	0	0	1
Address data	15	14	13	12	1	1	0
	11	10	9	8	0	1	0
	7	6	5	4	1	0	0
	3	2	1	0	0	0	0

Decimal equivalent codes (b) mode 3

Table 2 ML924 received PPM code interpretation, for modes 2 and 3

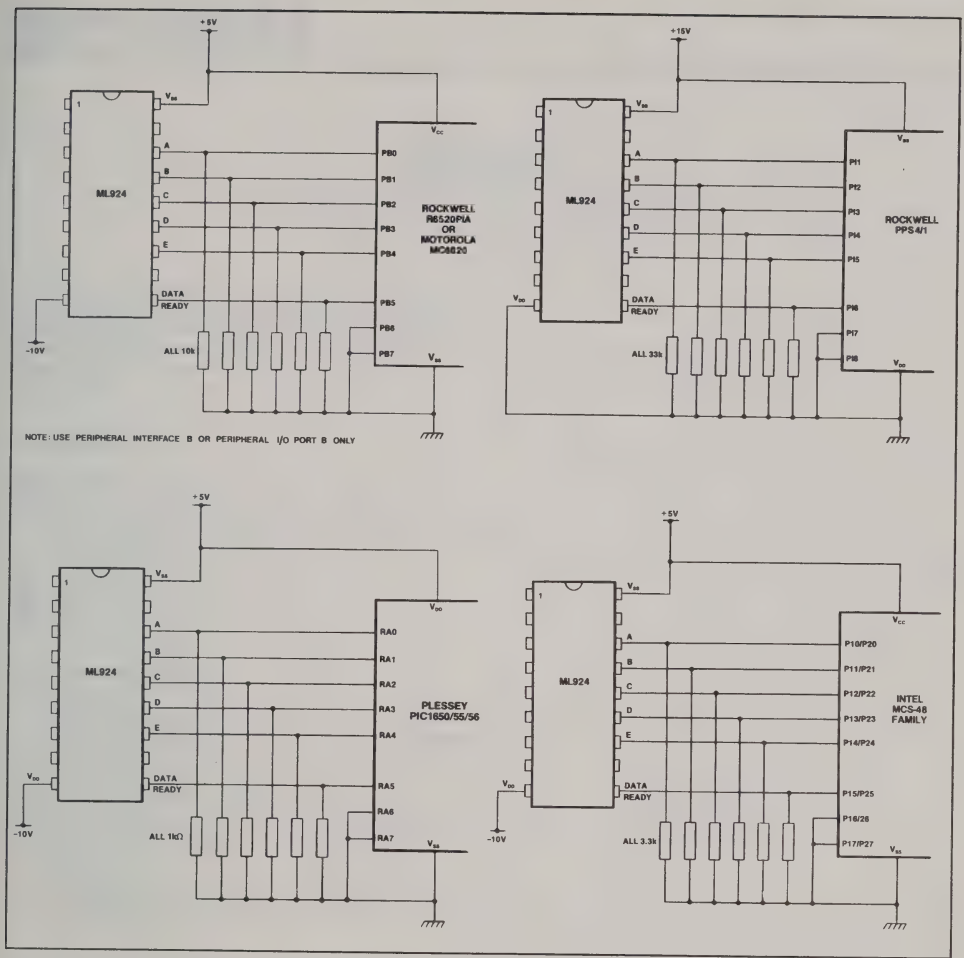


Fig.6 Interface to commonly used microprocessors

PLESSEY
Semiconductors

ML926/7
REMOTE CONTROL RECEIVERS
(With Momentary Outputs)

The ML926 and ML927 are MOS LSI monolithic circuits for use as receivers of remote control signals for television control and many other applications. They are general purpose devices each receiving sixteen of the thirty-two codes transmitted by the SL490 circuit as pulse position modulation (PPM).

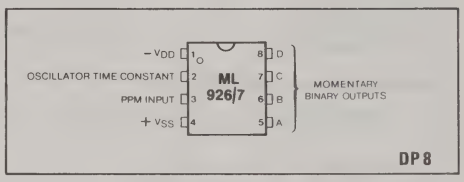


Fig.1 Pin connections top view

FEATURES

- Minimum Package Size – 8-Lead Minidip
- Four Outputs Indicate in Binary the Code Currently Being Received, and Are Switched Off (Low) When No Valid Code is Detected.
- On-Chip Oscillator
- High Power, Free Drain, Output Buffers

OPERATING NOTES

The receiver operates on a timescale fixed by an internal oscillator and its external timing components. The oscillator may be adjusted to any value between 15Hz and 150kHz (allowing different receivers to respond to different transmission rates withint the same area).

Checks are made to ensure 6 pulses, or 5 bits, are received for a word to be valid, and only after two consecutive and identical words is the receiver allowed to respond to the incoming code.

The ML926 responds only to codes 00001 to 01111 from the SL490 transmitter whereas the ML927 responds to codes 10001 to 11111.

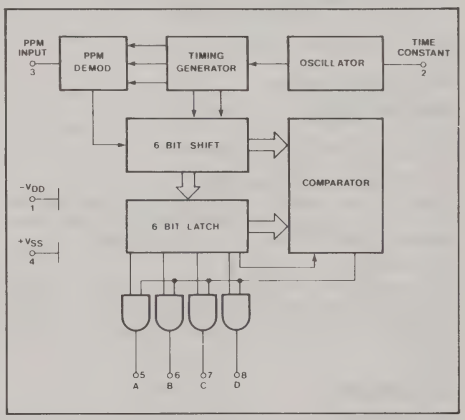


Fig 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

V_{DD} supply and inputs w.r.t. V_{SS}	+0.3V to –25V
Storage temperature	–55°C to +125°C
Operating temperature ambient	–10°C to +65°C

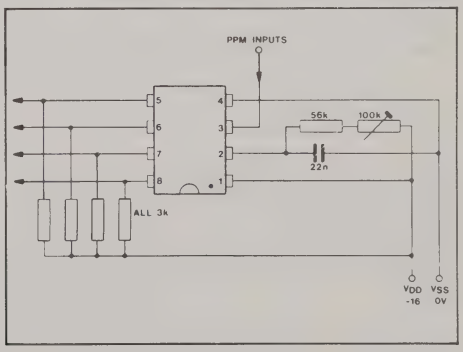


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
$V_{DD} = -16V$, $V_{SS} = 0V$
$T_{amb} = 25°C$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage range		12	14	18	V	
Current consumption	1	2	3	4	mA	
PPM input						
Input level high	3	−1		0	V	
Input level low	3	V_{DD}		−6	V	
Input pulse width	3	1		$22T_{osc}$	μsec	$T = \frac{1}{f_{osc}}$
Oscillator time constant See Note 1						
Oscillator frequency	2	15		150k	Hz	
			3k		Hz	Typical TC: 22nF to Vss
Variation wrt V_{DD}			1		%/V	100kΩ to V_{DD}
Output voltage high	5-8	-1.5		0	V	R_L = 3.0K to VDD
Output device leakage (Output OFF)	5-8			1	μA	

Note 1. R_{osc} (Pin 2) is 56k-156kΩ, $f_{osc} \simeq \frac{1}{0.15CR}$ ±20%

PIN FUNCTIONS

POSITIVE LOGIC '1' = Vss, '0' = V_{DD}

1. V_{DD}
−14V to −18V power supply

2. Oscillator time constant
An RC time constant of a capacitor and resistor at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz to 150kHz.

3. PPM input
The output of the 'front end' amplifier is connected to this pin; the signal must consist of a normal 'low' level with pulses to high level corresponding to the PPM pulses from the transmitter.

4. Vss
0V (ground)

5-8. A,B,C,D
Four open drain high power transistors give a binary coded output of the valid code being received.

	Momentary binary outputs	
Transmitter Code	ML926	ML927
E D C B A	D C B A	D C B A
0 0 0 0 0	0 0 0 0	0 0 0 0
0 0 0 0 1	0 0 0 1	↓ ↓ ↓ ↓
0 0 0 1 0	0 0 1 0	
0 0 0 1 1	0 0 1 1	
0 0 1 0 0	0 1 0 0	
0 0 1 0 1	0 1 0 1	
0 0 1 1 0	0 1 1 0	
0 0 1 1 1	0 1 1 1	
0 1 0 0 0	1 0 0 0	
0 1 0 0 1	1 0 0 1	
0 1 0 1 0	1 0 1 0	
0 1 0 1 1	1 0 1 1	
0 1 1 0 0	1 1 0 0	
0 1 1 0 1	1 1 0 1	
0 1 1 1 0	1 1 1 0	
0 1 1 1 1	1 1 1 1	
1 0 0 0 0	0 0 0 0	0 0 0 0
1 0 0 0 1	↓ ↓ ↓ ↓	0 0 0 1
1 0 0 1 0		0 0 1 0
1 0 0 1 1		0 0 1 1
1 0 1 0 0		0 1 0 0
1 0 1 0 1		0 1 0 1
1 0 1 1 0		0 1 1 0
1 0 1 1 1		0 1 1 1
1 1 0 0 0		1 0 0 0
1 1 0 0 1		1 0 0 1
1 1 0 1 0		1 0 1 0
1 1 0 1 1		1 0 1 1
1 1 1 0 0		1 1 0 0
1 1 1 0 1		1 1 0 1
1 1 1 1 0		1 1 1 0
1 1 1 1 1	↓ ↓ ↓ ↓	1 1 1 1

Table 1 Response to SL490 codes

PLESSEY
Semiconductors

ML928/9

REMOTE CONTROL RECEIVERS
(WITH LATCHED OUTPUTS)

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra-red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The ML928 and ML929 are general purpose remote control receivers, each receiving and latching 16 of the 32 codes transmitted by the SL490 circuit in the PPM (Pulse Position Modulation) mode. The ML928 responds to codes 00000 to 01111 only, and the ML929 to codes 10000 to 11111. Both devices are packaged in 8-lead minidip to minimise board area. The on-chip oscillator may be adjusted from 15Hz to 150kHz, allowing different transmission rates. They have a high degree of immunity to incorrect codes; there must be two consecutive correct codes received before the outputs can change.

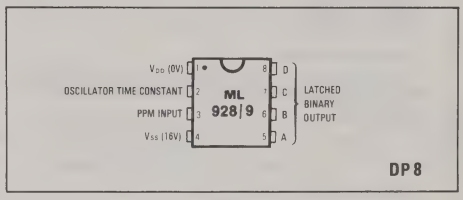


Fig.1 Pin connections - top view

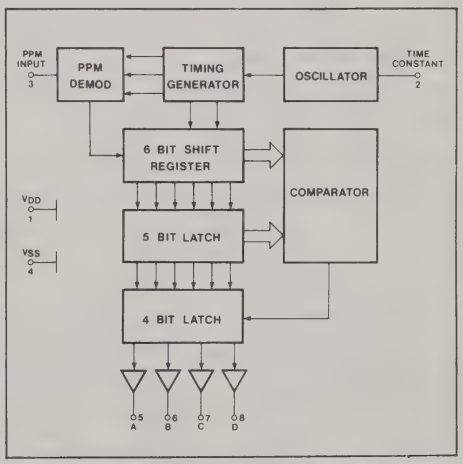


Fig. 2 ML928, ML929 remote control receivers block diagram

FEATURES

- Accepts 5 Bit PPM
- On-Chip Oscillator, 15Hz to 150kHz Range
- Easily Used With Ultrasonic, Infra-Red or Other Transmission Media
- Four High Drive Outputs
- 16 Latched States
- Minimum Sized Package

QUICK REFERENCE DATA

- Power Supply: 12V to 18V. Typical 4mA at 16V.
- Demodulation: Pulse position with time window checking by on-chip oscillator
- Decoder: 5 Bit with successive codeword comparison
- Outputs: Maximum 15mA sourced from open drain drive
- Logic convention: Logic 0 – output transistor ON, pulls output to V_{SS}
  Logic 1 – output transistor OFF

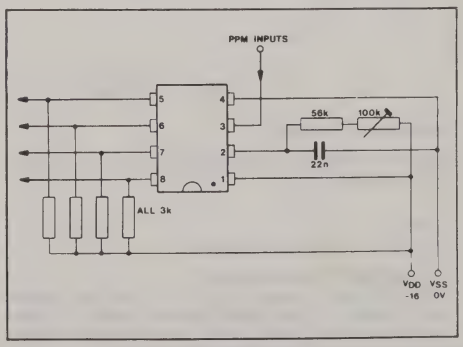


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{SS} = 0V$
$V_{DD} = -16V$
$T_{amb} = +25°C$

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Current Consumption V_{DD}	1	3	4	5	mA	
Supply voltage	1	−12		−18	V	
PPM input	3					
Logic '0' level		−1		0	V	
Logic '1' level		V_{DD}		−6	V	
Input pulse width		1		$22T_{osc}$	μs	$T_{osc} = \frac{1}{f_{osc}}$
Oscillator Timing	2					
Frequency		15		150k	Hz	
			3k		Hz	Typical TC: 22nF to Vss, 100kΩ to V_{DD}
Variation w.r.t. V_{DD}			1		%/V	
Latched binary output	5, 6, 7, 8	-1.5		0V	V	RL = 3.0k to VDD
Logic '0' output voltage						
Output leakage in logic '1' state				1	μA	

Note 1. $R_{osc.}$ (pin 2) is 56k-156k Ω. $f_{osc.} \simeq \frac{1}{0.15CR}$ ±20%

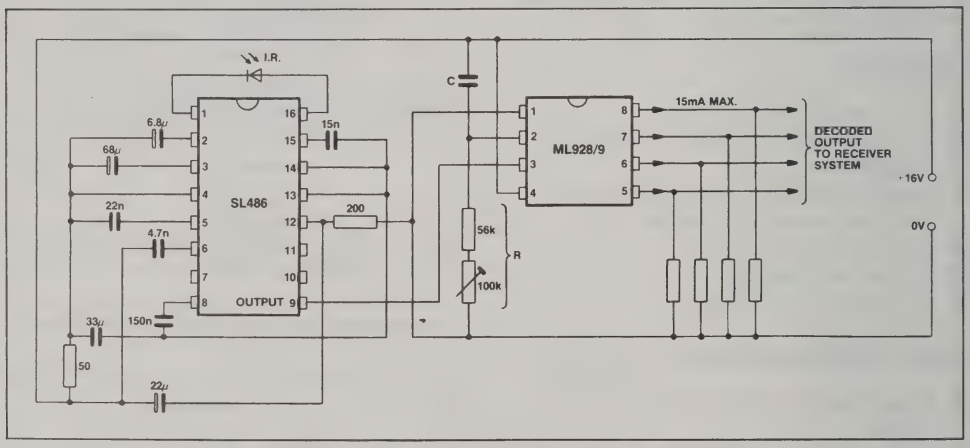


Fig.4 Typical application circuit, also shows general SL486 interface

PIN FUNCTIONS

Negative logic: '0' is 0V (V_{SS}), '1' is − 12V to −18V (V_{DD})

1. V_{DD}
−12V to −18V power supply

2. Oscillator time constant
An R-C time constant at this pin defines the internal clock frequency. The clock frequency may be varied from 15Hz at 150Hz and should be set so that there are 40 periods in one 't_o' transmitter pulse interval.

3. PPM input
The output of the 'front end' amplifier is connected to this pin; the signal must consist of a normal low level with pulses to high level corresponding to the PPM pulses from the transmitter.

4. V_{SS}
0V (ground)

5-8. A,B,C,D
Four open-drain high power transistors give a binary coded latched output of the last valid code received.

Transmitter Code	Latched binary outputs	
	ML928	ML929
E D C B A	D C B A	D C B A
0 0 0 0 0	0 0 0 0	
0 0 0 0 1	0 0 0 1	
0 0 0 1 0	0 0 1 0	
0 0 0 1 1	0 0 1 1	
0 0 1 0 0	0 1 0 0	
0 0 1 0 1	0 1 0 1	
0 0 1 1 0	0 1 1 0	
0 0 1 1 1	0 1 1 1	
0 1 0 0 0	1 0 0 0	No change
0 1 0 0 1	1 0 0 1	
0 1 0 1 0	1 0 1 0	
0 1 0 1 1	1 0 1 1	
0 1 1 0 0	1 1 0 0	
0 1 1 0 1	1 1 0 1	
0 1 1 1 0	1 1 1 0	
0 1 1 1 1	1 1 1 1	
1 0 0 0 0		0 0 0 0
1 0 0 0 1		0 0 0 1
1 0 0 1 0		0 0 1 0
1 0 0 1 1		0 0 1 1
1 0 1 0 0		0 1 0 0
1 0 1 0 1		0 1 0 1
1 0 1 1 0	No change	0 1 1 0
1 0 1 1 1		0 1 1 1
1 1 0 0 0		1 0 0 0
1 1 0 0 1		1 0 0 1
1 1 0 1 0		1 0 1 0
1 1 0 1 1		1 0 1 1
1 1 1 0 0		1 1 0 0
1 1 1 0 1		1 1 0 1
1 1 1 1 0		1 1 1 0
1 1 1 1 1		1 1 1 1

Table 1 Response to SL490 codes

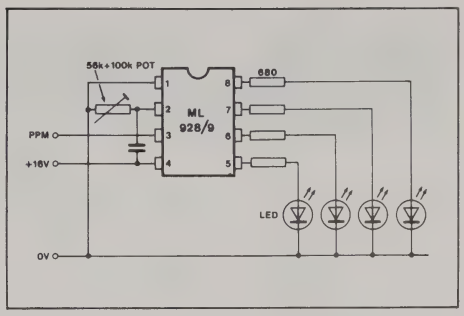


Fig. 5 Direct drive of LEDs

ABSOLUTE MAXIMUM RATINGS

V_{DD} supply and inputs w.r.t. Vss	+0.3V to −25V
Storage temperature	−55°C to +125°C
Operating temperature ambient	−10°C to +65°C

PLESSEY Semiconductors — ADVANCE INFORMATION — TELEVIEW

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MR9710

TELEVIEW DATA ACQUISITION CHIP

The MR9710 Data Acquisition (DA) chip is one of the set of LSI devices comprising the Plessey Semiconductor Teleview (Teletext/Viewdata) system. It receives data from a TV signal or Telephone Line via an appropriate interface and processes the data accordingly. Under instruction from a control device it acquires the requested data and loads it into the correct location in the preselected page store. Control information extracted from the incoming data is provided to the Teleview system.

The device is fabricated in Plessey Semiconductor N-channel metal gate MOS process providing direct TTL interfacing, high speed and good reliability. It is supplied in a 40 lead dual-in-line package.

FEATURES

- Processes Teletext and Viewdata Input Data
- Direct Interface with Teleview Highways
- Direct Interface with Standard UAR/T (MR1015)
- TTL Compatible Serial Teletext Data Input
- Full Checking of Teletext Data including Parity, Hamming and Data Frequency
- 'Don't Care' Digit Facility
- Non-used Viewdata Control Codes made available to Control Processor.
- Addresses Up To Eight Page Stores

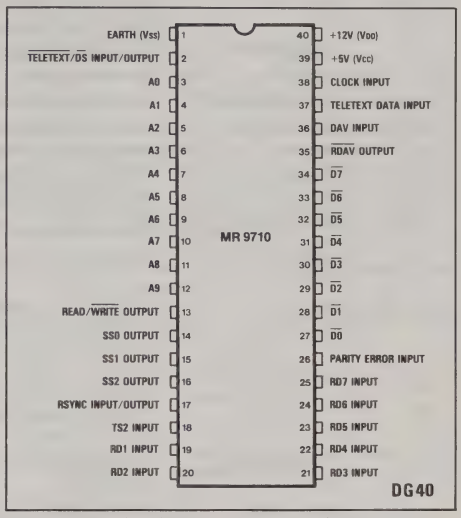


Fig.1 Pin connections - top view

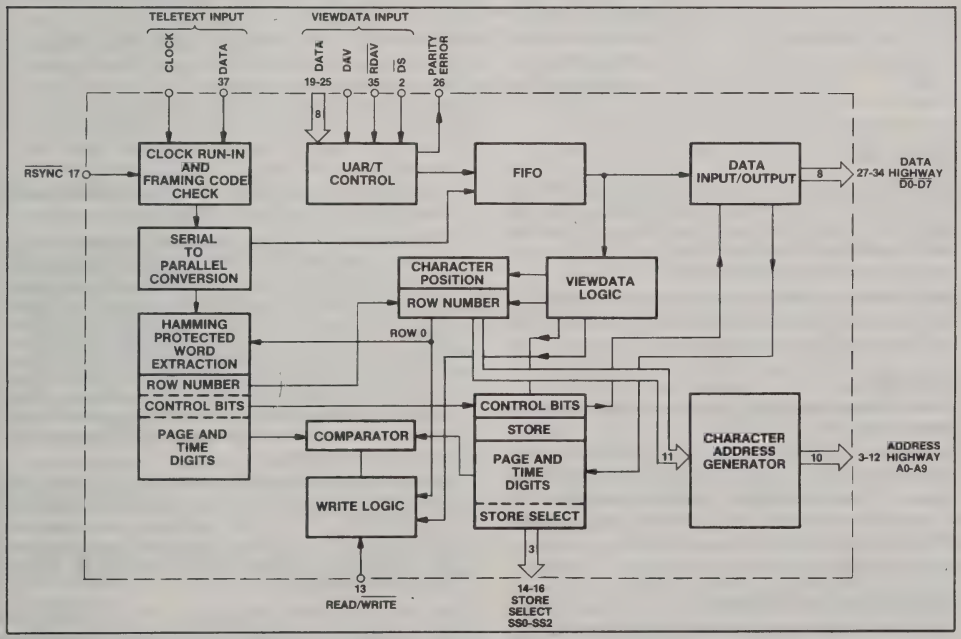


Fig.2 MR9710 block diagram

PIN FUNCTIONS

Pin Number	Name	Function
1	Vss	This is the negative supply for the device and the reference for all signals and electrical parameters.
2	$\overline{\text{TELETEXT}}/\overline{\text{DS}}$ INPUT/OUTPUT	When strapped to earth (low level), the DA chip will process Teletext. In Viewdata it is the data strobe output to the UAR/T (active low).
3–12	A0 to A9	The 10 bits of address connected to the Address Bus of the Teleview system. As outputs they are tristate and active push-pull for high speed driving the store. They are also inputs to enable the device to be addressed.
13	Read/$\overline{\text{Write}}$ Output	The read/write control of the page Stores. The Stores will output data (read) when this signal is high.
14–16	SS0–SS2 Outputs	Three bits of Store Select code enabling one of the eight page Stores.
17	$\overline{\text{RSYNC}}$ Input/ Output	A low going pulse indicates to the DA the start of a Teletext line. The DA will output a low going pulse within a few microseconds to re-synchronise the Data Grabber.
18	TS2 Input	The second of the two time slot bits which, when true, indicates that the DA may use the Data and address highways.
19–25	$\overline{\text{RD1}}$–$\overline{\text{RD7}}$ Inputs	Received Data taken directly from the UAR/T.
26	Parity Error Input	The Parity error signal from the UAR/T.
27–34	$\overline{\text{D0}}$–$\overline{\text{D7}}$	Data I/O's for connection directly to the Teleview Data highway. As an output the active state is low and there is a passive pull-up on chip so that the signals on the highway may be 'wire-ored'.
35	$\overline{\text{RDAV}}$ Output	Low active signal to the UAR/T which will reset its data available output.
36	DAV Input	The Data Available signal from the UAR/T to indicate a character is available at the RD1–RD7 pins.
37	Teletext Data Input	Serial data input from a Data Grabber. TTL compatible. If not used this input should be held low.
38	Clock Input	Normally the Teletext clock running at 6.9375 MHz and synchronised to the Teletext data by $\overline{\text{RSYNC}}$. In Viewdata only applications a 6MHz clock as used by the Video generator may be input here. TTL compatible.
39	Vcc	Connected to +5V. This has a low current requirement and is used mainly for the output drivers.
40	Vdd	Connected to +12V, the main positive supply for the device.

OPERATION

The Data Acquisition (DA) chip takes data from either the TV (Teletext) or telephone line (Viewdata) via the appropriate interface, processes it accordingly to type and user requests and loads the display data in the correct position in one of eight page Stores.

The processing of Teletext and Viewdata information is described in separate sections as is the interchange of data with the rest of Teleview system.

TELETEXT

If pin 2 is held low the DA may receive data via the serial Teletext data input.

While TS2 is true the DA will monitor $\overline{\text{RSYNC}}$ and the address highways. If a pulse appears on $\overline{\text{RSYNC}}$ it will process a Teletext data-line. At other times while TS2 is true it will respond to signals on the address highway and interchange data with a Control Device.

While TS2 is false the DA will do nothing.

TELETEXT DATA RECEPTION

Data is extracted from the TV video signal by an external circuit called the Data Slicer. This circuit provides a serial data signal and a clock to the DA's input.

A 0.5μsec negative pulse generated by the MR9735 Video Generator will appear on the $\overline{\text{RSYNC}}$ line just before the data on a possible Teletext line. This pulse stops the clock in the low state and primes the MR9710 to monitor the Teletext Data Input for clock run-in. The first negative transition restarts the clock which is used as a reference against which to compare the incoming signal. If the frequency is correct the MR9710 outputs a second $\overline{\text{RSYNC}}$ pulse which allows accurate resynchronisation of the clock for the rest of the Teletext line. If the frequency check fails the MR9710 goes back to its idle state waiting for a new $\overline{\text{RSYNC}}$ signal or the Data Interchange time.

After a valid clock run-in has been detected Teletext data is clocked into a serial to parallel converter and Framing Code detector. A time out will cause DA to go idle, while the detection of Framing Code will byte synchronise the S–P converter and start the DA receiving the Teletext data as shown in Fig.3.

The first two words following the Framing Code have data protected by Hamming Code and the appropriate

checks and corrections are performed. If the row address indicates that the data is a Page Header (Row 0) then the following 8 words are also processed by the Hamming Code circuit. If any Hamming Code fails such that it cannot be corrected, then that data line is rejected.

Requests for pages of Teletext data are input to the DA during the Data Interchange periods, described later. When a new page is selected the Page and Time store in the DA is loaded with all '1's indicating "don't care" digits. As keys are pressed by the user of the Teleview system the values are loaded into the DA in the appropriate position.

A comparator in the DA compares Magazine, Page and Time digits one at a time as they are received in the data stream with the digits stored. The comparator will give a true output if the digit compares exactly or if the stored digit is all 1 (value 15). Where an incoming digit has a range less than 4 bits, e.g. time hours tens has the range 0–3 or 2 bits, the unused bits will be made to compare.

Every line of data received is checked for comparison on Magazine number. If this does not compare and the row address indicates that the row is not a Page Header then that row is rejected.

If the Magazine number does not compare and it is a Page Header then, with the exception of Rolling Headers, it is again rejected.

From the time that the DA is told that the P key has been pressed until the selected page has been captured for the first time all Page Headers that compare on Magazine number are loaded into the Store except those with the Interrupted Sequence bit (C9) set. This mode of display is referred to as Rolling Headers and provides an indication to the user that data is being received. During this mode the Magazine Serial bit (C11) will over-ride the Magazine comparison. A page of data may be captured when the page number has been fully entered, i.e. the 3rd digit has been received or the T key has been pressed, and a Page Header is received whose Magazine, page and time digits compare with those stored in the DA. That header and all subsequent data lines with correct Magazine number will be stored up to and excluding the next Page Header of correct Magazine number. A 'Page being received' indication will be set at this time for transmission to the Control device.

Whenever a Page Header is received that fully compares the Control bits accompanying that Header will be stored for subsequent transmission to the Control.

When the content of a data line is ready to be stored that data is loaded into the appropriate Store as defined by the signal from the Control device. Its position in the Store is defined by the Row Address of that data line, the location of the first character being 40 times the Row Address (with the exception of the Page Header which does not have the first 8 characters), with following characters being stored in the next 39 locations of Store.

Each character is checked for odd parity and if the check fails that character is not written. The write signal is removed to avoid overwriting a possible valid character already existing in Store.

The last eight characters of every Page Header contain the current clock time and are always written to Store.

VIEWDATA

With pin 2 connected to the Data Strobe input to a UAR/T and not held to earth the DA will process Viewdata.

While TS2 is true the DA is active as far as the Teleview highways are concerned and it will monitor $\overline{\text{RSYNC}}$ and the Address highway.

When an $\overline{\text{RSYNC}}$ pulse appears the DA will process any Viewdata character it has available. Whenever it is not processing characters it may receive characters asynchronously from the telephone line, via the exclusive connection to the UAR/T, and store them within the DA. Up to three characters may be received and stored before the next processing period when they may be loaded into the page store. Data Interchange with the Teleview system may occur when TS2 is high.

VIEWDATA CHARACTER PROCESSING

The eight bit input consists of seven bits of data plus a parity fail indication. The codes are shown in Fig. 4.

Characters intended for storage are loaded into the Store in a location determined by the Character Address counter which is always arranged to point to the position in Store into which the next character will be written. The counter is manipulated by the Control Characters appearing in Cols. 0 and 1 in the character table.

0/ 8, Back Space, will cause the Character Address counter to be decremented by one.

0/ 9, Horizontal Tab, will cause the Character Address counter to be incremented by one.

0/10, Line Feed, will increment by 40.

0/11, Vertical Tab, will decrement by 40.

0/12, Form Feed, will reset to zero.

0/13, Carriage Return, will position the Character Address counter to the beginning of the current block of 40.

0/14, Cursor Home, will reset to zero.

A character in columns 2–7 will be written into the appropriate Store at the location indicated by the Character Address counter which will then be incremented by one.

The ESC character (1/11) will cause some modification of the following character as follows:–

If the character is in cols. 4 or 5 it will be written to Store with the most significant bit changed to Zero.

If the character is in col. 3 it will not be written to Store but made ready for transmitting to the Control device.

Any other characters, except NUL, will cancel the ESC sequence and be ignored.

The Form Feed character (0/12) will cause the F bit to be set in the appropriate DA to Control signalling word.

All other control characters in cols. 0 and 1, except NUL, will be sent to the Control at the appropriate time.

If any character has the parity fail indication set then the character 7/15 will be written to Store. At the start of a processing period (i.e. at $\overline{\text{RSYNC}}$) if a character is available for processing then the DA will erase the Cursor bit by reading the location pointed to by the Character

ASYNCHRONOUS DATA RECEPTION

The standard UAR/T (MR1015D), will convert the serial data received via the modem to parallel data for inputting to the DA and indicate a character is ready by the data available (DAV) line. At any time, except when actually processing previously received characters, the DA will read the data and acknowledge on $\overline{\text{RDAV}}$, a minimum of 3μsec after the DAV signal.

Address counter and re-write it. Since the DA never writes the 8th bit in the Store the cursor will be removed.

DATA INTERCHANGE

During the DA's active period, indicated by TS2, when it is not performing any data processing then it will monitor the Address highway for the following codes:

1111XXXX0X	indicates the DA should receive data from the data highway.
1111XXXXX0	indicates that the DA should send data to the data highway.
1111X0XXXX	indicates that the DA should provide control to the UAR/T.

In the Receive mode the Control device may send data according to the codes in Table 1. The most significant bit of the data acts as a strobe which will cause the other 7 bits to be received and stored in the DA. Magazine, Page and Time digits will be stored in the appropriate location in the digit store, the Store Select number will be stored for use when accessing the Store and the indications of P and T keys being processed will also be latched for use in the processing period.

The receiving of data from the Control is completely asynchronous to the DA's internal clock and is controlled entirely by the Strobe bit.

The Send mode will cause the DA to apply the first code, shown in Table 2, to the data highway. When the code has been read by Control the signal will be acknowledged by Control forcing all 1's (low levels) which will step the DA onto the second word and so on. The Strobe bit is used in this case to indicate that the data is appearing for the first time and once read by Control, is cleared until new data is available. The exception is the first word which always has the Strobe set.

The UAR/T control is recognised by the DA since it has the UAR/T connections and in this mode a Strobe on the data highway will cause the DA to provide a data strobe $\overline{DS}$ to the UAR/T.

During the Data Interchange period the DA will monitor the Store Select lines and if they are all taken low it will output the current content of the Character Address counter to the address highway so that the Control may know where to insert the cursor.

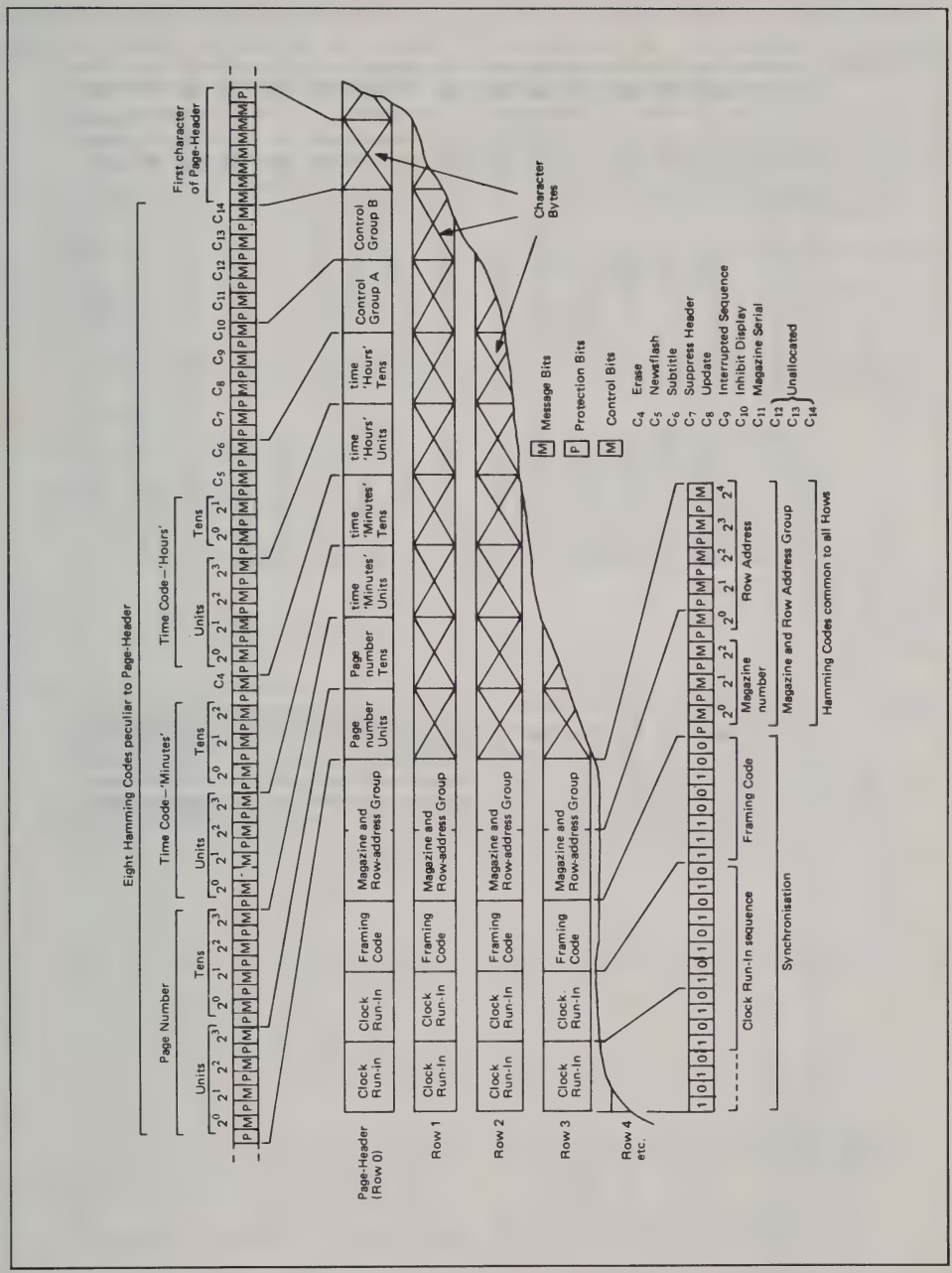
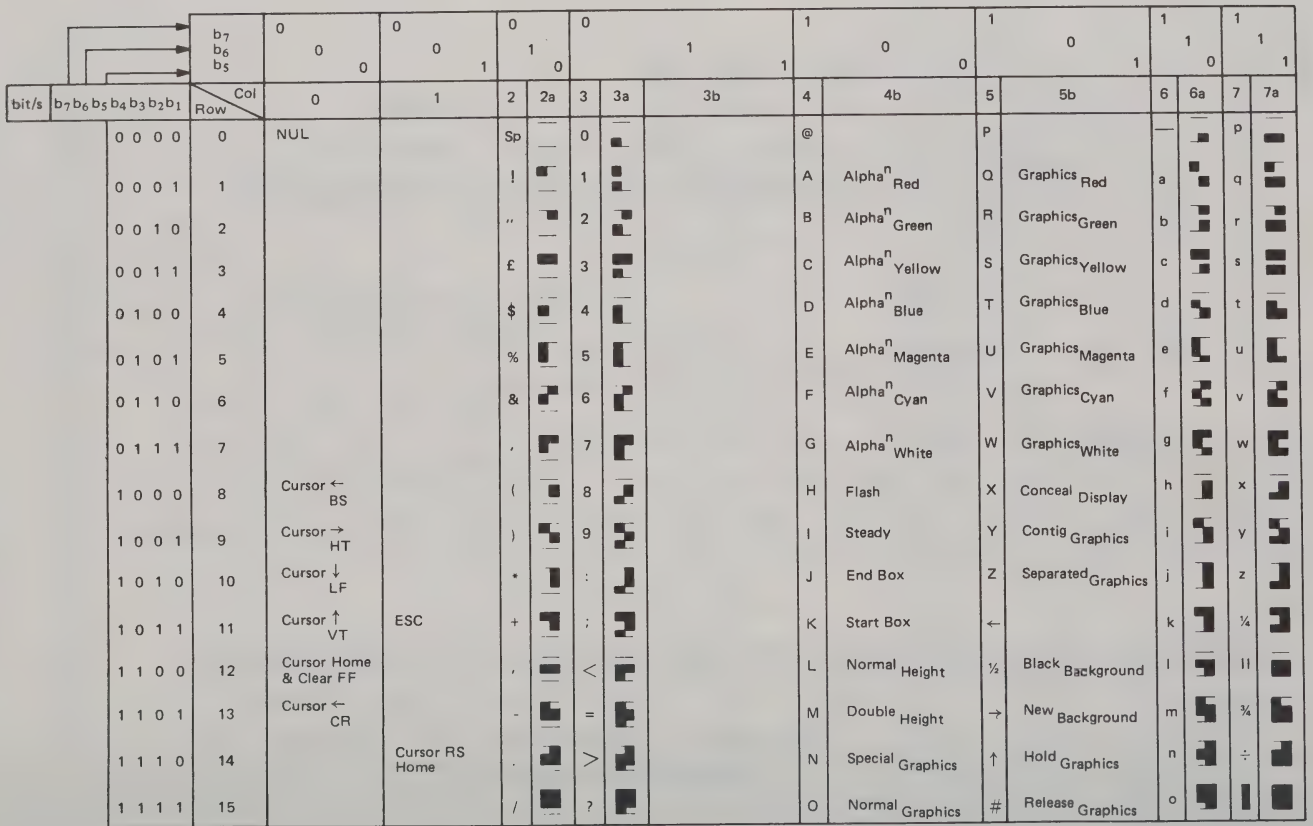


Fig.3 Synchronisation and Hamming codes at start of page-header and row transmission



bit/s $b_7 b_6 b_5 b_4 b_3 b_2 b_1$	Row \ Col	0	1	2	2a	3	3a	3b	4	4b	5	5b	6	6a	7	7a
		b_7 b_6 b_5 0 0 0	0 0 1	0 1 0		0 1 1			1 0 0		1 0 1		1 1 0		1 1 1	
0 0 0 0	0	NUL		Sp		0			@		P		—		p	
0 0 0 1	1			!		1			A	Alpha^{n} Red	Q	Graphics Red	a		q	
0 0 1 0	2			"		2			B	Alpha^{n} Green	R	Graphics Green	b		r	
0 0 1 1	3			£		3			C	Alpha^{n} Yellow	S	Graphics Yellow	c		s	
0 1 0 0	4			$		4			D	Alpha^{n} Blue	T	Graphics Blue	d		t	
0 1 0 1	5			%		5			E	Alpha^{n} Magenta	U	Graphics Magenta	e		u	
0 1 1 0	6			&		6			F	Alpha^{n} Cyan	V	Graphics Cyan	f		v	
0 1 1 1	7			'		7			G	Alpha^{n} White	W	Graphics White	g		w	
1 0 0 0	8	Cursor ← BS		(		8			H	Flash	X	Conceal Display	h		x	
1 0 0 1	9	Cursor → HT		)		9			I	Steady	Y	Contig Graphics	i		y	
1 0 1 0	10	Cursor ↓ LF		*		:			J	End Box	Z	Separated Graphics	j		z	
1 0 1 1	11	Cursor ↑ VT	ESC	+		;			K	Start Box	←		k		¼	
1 1 0 0	12	Cursor Home & Clear FF		,		<			L	Normal Height	½	Black Background	l		II	
1 1 0 1	13	Cursor ← CR		-		=			M	Double Height	→	New Background	m		¾	
1 1 1 0	14		Cursor RS Home	.		>			N	Special Graphics	↑	Hold Graphics	n		÷	
1 1 1 1	15			/		?			O	Normal Graphics	#	Release Graphics	o			

Fig 4 Viewdata transmission codes recognised by the MR9710

CONTROL TO DATA ACQUISITION SIGNALLING

Active low signalling, most significant bit is a strobe.

Highway Free		0000 0000
Magazine Number		1000 Dddd
Page Number,	tens	1001 Dddd
	units	1010 Dddd
Store Select		1011 0Sss
Key Pressed		1011 10Kk
Spare Code		1011 1100
Spare Code		1011 1101
Spare Code		1011 1110
Dummy Code		1011 1111
Time Hours,	tens	1100 Dddd
	units	1101 Dddd
Minutes,	tens	1110 Dddd
	Units	1111 Dddd

Where Kk is key identification:

P	00
T	01
Spare 1	10
Spare 2	11

Table 1

Sss is store select number, 000 to 111.

Dddd, Digit key value, initially values 0–9 and 15 used although any value may be sent. For Teletext the magazine range is 0–7, Time hours tens range 0–3, Time minutes tens range 0–7. In addition digit 15 is recognised by the DA as a 'don't care' digit causing automatic comparison.

DATA ACQUISITION TO CONTROL SIGNALLING

Active low signalling, most significant bit is a strobe. Signals acknowledged by the Control forcing all ones. Control word 1 is sent first and is always sent.

Control word 1	1000	T	S	s	s	
Where T	is the Teletext bit, 1 = Teletext.					
S s s	is the Store Select number the DA is currently using.					

Control words 2–4 depend on whether Teletext or Viewdata is being processed.

TELETEXT

Control word	2	1001	PBR	C4	C6	C5
	3	1010	C10	C9	C8	C7
	4	1011	C14	C13	C12	C11

Sent* only when Valid Header received.

PBR is set while a page is being received.

C4 to C14 are the Teletext Control bits.

VIEWDATA

Control word	2	1001	X	F	0	0
	3	1010	b7	0	b6	b5
	4	1011	b4	b3	b2	b1

Sent* only when a Control character received by DA.

F is set when Form Feed character processed.

b1–b7 are the 7 bits comprising the Viewdata Character.

Table 2

***NOTE**: that 'sent' means the Strobe bit is set. The other seven bits are actually put onto the highway at the request of the Control and may be used if appropriate (page being received, for example).

PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{CC} Power Supply (V_{CC})	+5V Supply
2	NC	Not connected
3	Ground (V_{GD})	0V connection and Logic I/O reference level.
4	Received Data Enable ($\overline{RDE}$)	A logic '0' on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when $\overline{RDE}$ is '0' and a high impedance state when $\overline{RDE}$ is '1'. Thus, the data output lines can be bus structure oriented.
13	Parity Error (PE)	This line goes to a logic '1' if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error (FE)	This line goes to a logic '1' if the received character has no valid stop bit. Tri-state.
15	Over-Run (OR)	This line goes to a logic '1' if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	Status Word Enable ($\overline{SWE}$)	A logic '0' on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	Reset Data Available ($\overline{RDAV}$)	A logic '0' will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data Available (DAV)	This line goes to a logic '1' when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig.14.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic '1') to spacing (logic '0') transition is required for initiation of data reception. Figs.13 and 14.
21	External Reset (XR)	Resets all registers except the control bits register. Sets SO, EOC, and TBMT to a logic '1'. Resets DAV, and error flags to '0'. Clears input data buffer. Must be tied to logic '0' when not in use.
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer empty flag goes to a logic '1' when the data bits holding register may be loaded with another character. Tri-state. See Figs.20 and 22.
23	Data Strobe ($\overline{DS}$)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS. Data must be stable during entire strobe.
24	End of Character (EOC)	This line goes to a logic '1' each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Figs.19 and 21.
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic '1' when no data is being transmitted. See Figs.7, 8, 9 and 10.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available.
34	Control Strobe (CS)	A logic '1' on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic '1' level.
35	No Parity (NP)	A logic '1' on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic '0'.
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic '0' will insert 1 stop bit and a logic '1' will insert 2 stop bits. The combined selection of 2 stop bits and 5 bits/character will produce 1½ stop bits.
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic '0' will insert odd parity and a logic '1' will insert even parity.
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud.

PLESSEY
Semiconductors

MR9735

TELEVIEW 625 LINE VIDEO GENERATOR

The Video Generator Chip is one of a set of LSI chips used in the Plessey Semiconductor TELEVIEW Teletext/Viewdata system. It reads the contents of a Page Store and generates outputs suitable for driving a normal 625 line Colour Television receiver to display the contents of the Page Store.

The chip also monitors the composite synchronising signals within the receiver and locks the total TELEVIEW system onto the incoming interlaced signals. When no transmission is taking place the chip generates an interlaced or non–interlaced composite sync. signal which is used to synchronise the receiver.

A full set of colour display facilities as described in the Broadcast Teletext Specification (September 1976) is provided by the device.

The device is fabricated in Plessey Semiconductors N-Channel metal gate MOS process providing direct TTL interfacing, high speed and good reliability.

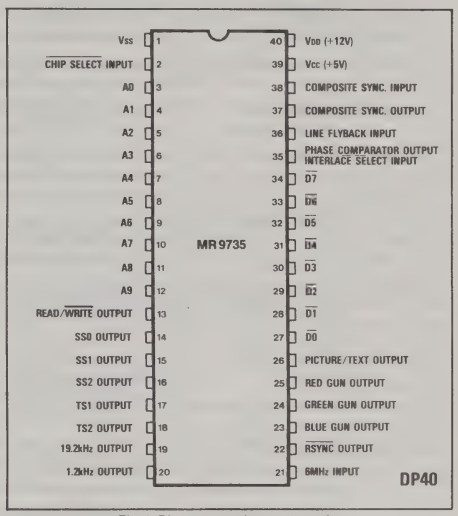


Fig.1 Pin connections - top view

FEATURES

- Interlaced 625 line or non-interlaced 313 line operation
- 24 Row x 40 Character display
- Character Set options available
- On and Off Hours operation
- Half Page Expansion
- Boxed Clock and Header on Teletext
- Direct interfacing with the TELEVIEW busses
- Provides master timing signals for the other TELE-VIEW chips to indicate the status of the display scan.
- Can address up to eight Page Stores
- Provides the address information to scan the allocated Page Store
- Provides composite synchronising signals for the receiver for 'Off-Hours' working
- Provides comprehensive set of display facilities
- Can receive Teletext on lines 7-22

DISPLAY FACILITIES

1. Provides the following display facilities controlled by 'control' characters read from the store i.e. via the TELETEXT/VIEWDATA transmission.

(a) Alpha-numerics/Graphics in seven colour set.

(b) Colour or black backgrounds.

(c) Selected characters can be concealed.

(d) Selected characters can be flashed.

(e) 'Boxed' characters can be inserted into the normal Television Picture. This can be done manually or automatically.

(f) Characters may be either single or double height.

(g) Graphics characters may be contiguous or separated.

(h) Graphics characters may be 'held' during other control characters.

(i) Special graphics for high resolution applications, a dynamically redefinable character set application also available.

2. Provides the following display facilities controlled from the users keyboard/keypad via the control chip (e.g. PIC1650-532).

(a) Switch between normal and data video.

(b) Teletext or Viewdata Operation.

(c) Clock time can be boxed into a normal picture (Teletext only).

(d) Display of one half of a page in double height.

(e) Black and white output of data in Mix Mode.

(f) Inhibiting of character rounding and flashing.

(g) Enabling of a cursor.

(h) Inhibit the display until updated.

(i) Reveal 'concealed' characters.

CHARACTER SETS

English	MR9735-002
German	MR9735-003
Swedish/Finnish	MR9735-004
Danish	MR9735-005
Italian	MR9735-006
Others	Contact Factory

PIN FUNCTIONS

Pin Number	Name	Function
1	Vss	This is the negative supply for the chip and is used as a reference for all the electrical parameters.
2	$\overline{\text{Chip Select}}$ Input	The chip can be put in its deselected state by connecting this input to Vcc. The input has an internal pull down to Vss. If connected to Vdd the test mode is selected.
3-12	A0-A9	These pins are connected to the Address Bus of the TELEVIEW system. They are used for address Input/Output.
13	Read/$\overline{\text{Write}}$ Output	This output is used to drive the Random Access Memories forming the Page Memory.
14-16	SS0-SS2 Outputs	These binary coded outputs are used to select the required Page Store.
17,18	TS1,TS2 Outputs	These outputs are generated by the Video Generator from the status of the raster scan and are used to indicate this status to other chips within the TELEVIEW system.
19,20	19.2kHz and 1.2kHz Outputs	These outputs provide 19.2kHz and 1.2kHz square wave signals which are used by the UAR/T as reception and transmission clocks respectively.
21	6MHz Input	This input is fed from a 6MHz oscillator which is phase locked to the normal transmission for Teletext ON Hours operation. During OFF Hours working a free running crystal oscillator is normally used.
22	$\overline{\text{RSYNC}}$ Output	This output is an open-drain output and is used to indicate the presence of Teletext lines to the Teleview D.A. Chip MR9710 and Data Slicer SL9100. The timing of this signal is indicated in Fig.9.
23-25	Red, Green and Blue Outputs	These outputs are push-pull outputs which go high to turn on the relevant colour gun for displaying. These outputs are closely matched for propagation delay and rise and fall times.
26	Picture/$\overline{\text{Text}}$ Output	This output may be used by the TV receiver to determine whether to display the normal TV Picture or the generated Text as provided at the Red, Green and Blue outputs. In the mix mode this generates monochrome video. It will then be matched to the gun outputs for propagation delay and rise and fall times.
27-34	$\overline{\text{D0}}$-$\overline{\text{D7}}$ Inputs	The Data Inputs form the communication highway between the Video Generator and the Control Processor and Page Memory.
35	Phase Comparator Output/Interlace Select Input	In on-hours operation the display Line Flyback signal is compared for phase with an internal 64μs period signal derived from the 6MHz display clock. The output is a pulse which produces a voltage for controlling the frequency of a 6MHz display oscillator, thus locking the display to the incoming picture. In off-hours operation this open drain output goes high permanently, and thus can be used as an indication of on-hours/off-hours status. When this output is high the oscillator must run fast and when this output is low the oscillator must run slow. In OFF Hours operation if the Phase Comparator output is held low a 313 line non-interlaced sync. is provided at the Composite Sync. output. If the Phase Comparator output is pulled high connected to Vcc via a 4.7k resistor interlaced sync. will be provided.
36	Line Flyback Input	The Line Flyback input is a signal from the display deflection circuitry which is used for positioning the display on the T.V. screen. Line Flyback pulses are positive. If no Line Flyback is provided in OFF hours mode the display will be positioned so that the start of video is approximately 16μs after the negative edge of line sync.
37	Comp. Sync. Output	This output is an open drain output. In on-hours working or in Picture mode it outputs a regenerated composite sync. signal from the comp. sync. input. In off-hours working it outputs an internally generated composite sync.
38	Comp. Sync. Input	The Composite sync. input monitors the composite sync/video being received and extracts synchronising information and 'on-hours' 'off-hours' information for the Video Generator. This input must be predominantly high for 'off-hours' switching. Sync. pulses are negative.
39	Vcc	This pin is connected to the +5.0V supply.
40	Vdd	This pin is connected to the +12.0V supply.

CHIP DESCRIPTION

The Video Generator Chip contains the logic and control functions to interrogate a selected TELEVIEW Page Store and display the contained information at the correct period within the raster scan on a normal TV receiver. The chip also generates the master timing signals TS1 and TS2 which indicate the raster status to the Control processor and Data Acquisition chips.

The basic block diagram of the chip is shown in Fig.4 and major functional blocks are described below.

1. Comp Sync Generator and On Hours Detector

The prime function of this block is to detect negative going sync. signals from the incoming mixed sync. and to synchronise the TELEVIEW system with the transmitted signal. When the incoming transmission is turned off, (i.e. goes 'Off-hours'), this is recognised by the detector after at least 300ms of missing sync. pulses. An internally generated Composite Sync signal is then switched to the Composite Sync Out pin. Thus the receiver will continue in lock but synchronised to the Video Generator. Similarly if the normal transmission resumes, the fact that external sync pulses are being received is recognised by the Video Generator and the chip will re-synchronise itself with the incoming transmission. Because the Video Generator is aware of the status of the mixed sync. at all times the chip can detect frame sync., line sync. and even or odd frames. Thus with this information the chip can continuously monitor the current line number. The relevant sections of the line scan are decoded and are indicated externally by the TS1, TS2 time slot outputs. These signals are fully described in Figs.7 and 8, but there are four periods i.e.

(i) Writing to RAM. TS10
This occurs during lines 7 to 22 under control of the D.A. chip.

(ii) Reading from RAM. TS00
This occurs under control of the Video Generator chip between lines 48 and 288, and is when the display is active.

(iii) Data Interchange Period. TS11
The Interchange of information between D.A., Control Processor and Video Generator occurs during this period (lines 23–47).

(iv) Spare TS01
During lines 289–296 the Video Generator does not use the Data Bus.

As the chip is aware of the raster status the chip also starts and stops the address counter/latch combination which is used to scan the relevant Page Memory. The form of the generated sync. pulses are shown in Fig. 5.

2. Character Counter and Address Logic

The address counter is a binary counter which is incremented at the Character Display Rate (1MHz). It can also be loaded from a latch which contains the start address of each character row. Since each character consists of 10 vertical lines of raster scan, the counter is incremented 40 times from a start address and then is reloaded with the same start address ready for the next raster scan of the same forty characters. This occurs nine times. On the last line the counter is incremented an extra once and this new address is stored in the latch. This address being the start address of the next row of forty characters. The above sequence is then repeated.

If displaying only one half of a page with all characters in double height, the Video Generator scans the same forty addresses nineteen times and stores the new address on the twentieth raster scan. If it is in the bottom half of the page, the address counter is initialized to 480.

The display format of 40 characters, each 1μs wide, occurs on a line of 64μs duration thus leaving a border of 12μs at each end of the character row. This address counter is actually started some 4μs before the start of the proper character display thus allowing time for address generation, RAM access time, ROM access time and display processing, these actions being pipelined. Facilities are also provided such that the output address can be reduced by 40 thus allowing accessing of the character in the row above. This is a necessary operation for a 'Double Height' display option which will be described later. This facility is inhibited while displaying one half of a page. The address so produced is presented on the address bus and the required Page Memory is activated by the Store Select Outputs. The address drivers are tristate thus allowing easy bus interface, being active for 40μs starting 3.5–6μs after LFB.

3. Input Latches and Character Read-Only Memory

The data being read from the required Page Memory is placed on the Data Bus and is latched into the Data Bus latches. A total of 450ns is allowed for the RAM read cycle and thus quite slow Random Access memories may be used. Having been latched by the Video Generator chip the seven bit character is used to address the character Read Only Memory. This memory is organised as 96 characters each of 45 dots (5 x 9 array).

4. Data Control Latches (Colour Background Control)

Certain characters indicate to the video generator a change in display status. These characters are contained within columns 0 to 1 of the character set as shown in fig. 7 and may be used to change character colour, background colour, height, etc. These facilities, and the control of them, are fully described in the British Broadcasting Teletext Specification (Sept. 1976) published by the BBC, IBA and BREMA.

5. Output Logic and Drivers

The output logic reads the character ROM into a six bit parallel to serial shift register. This operation occurs at the left-hand side of the character to be displayed, the data in the register is then shifted out at 6MHz (character dot-rate) the data bits selecting between character and background information. This information is used to drive the fast Gun output drivers. These outputs are closely matched for propagation delay and rise and fall time to ensure good legibility.

DATA INTERCHANGE

During the TS11 timeslot the Video Generator can receive information from other devices attached to the TELEVIEW system busses. This is normally used by the control chip to update the control and display latches within the Video Generator. The Video Generator is enabled to receive by putting the address 1111XXOXXX on the address highway (active high).

The latches are updated by the following control words, active low signalling, most significant bit is a strobe.

Highway Free	0	0	0	0	0	0	0	0	
Control Word 1	1	0	0	0	T	S	s	s	
Control Word 2	1	0	0	1	X	C_4	C_6	C_5	Teletext
Control Word 3	1	0	1	0	C_{10}	C_9	C_8	C_7	Teletext
Control Word 4	1	0	1	1	C_{14}	C_{13}	C_{12}	C_{11}	Teletext
Control Word 2	1	0	0	1	X	F	0	0	Viewdata
Control Word 3	1	0	1	0	b_7	0	b_6	b_5	Viewdata
Control Word 4	1	0	1	1	b_4	b_3	b_2	b_1	Viewdata
Store Select for Display	1	1	0	0	SP	D	d	d	
Key Data	1	1	0	1	*	P	*	*	
Other Facilities	1	1	1	0	X	BH	M	BC	

The Control bits are as follows:—

T	TELETEXT MODE i.e. NOT VIEWDATA
Sss	Identification of Store being written to
Ddd	Identification of Store being displayed from

(a) Teletext

C_4	Erases rows 1–23 of Store defined by Sss and resets Reveal if Sss = Ddd
C_5	Newsflash
C_6	Subtitle
C_7	Suppress Header
C_8	Update Indicator
C_9	No action
C_{10}	Inhibit display
C_{11}	No action
C_{12}–C_{14}	No action (may be programmed to enable and disable the chip)

(b) Viewdata

b_7–b_1	Cursor Control Bits
001 0001	Cursor ON } The two Control Words that make up these codes must be transmitted in numerical order in the same TS11 timeslot.
001 0100	Cursor OFF }
F	Form feed or first appearance, Erases store defined by Sss, resets Reveal if Sss = Ddd
SP	Sets Picture/Text to picture (for initialization)
P	P Key pressed. Resets Reveal, Half Page Expansion, Newsflash/Subtitle (Auto Box), Suppress header, Inhibit display, Update.
M	Mix Mode } The latches are set and reset by the appropriate bit
BC	Box Clock (Teletext only) }
BH	Box Header (Teletext only) }
***	These are coded as follows:–
001	Picture/Text Key pressed } Latches toggled by the appropriate code
010	Reveal/Conceal Key Pressed }
011	½ Page Key Pressed (Cycles Full, Top, Bottom, Full etc). }
100	Update/Clear Key pressed }
101	Rounding and Flashing OFF (Reset by P Key or new viewdata page)
111	Hold (not used by MR9735)

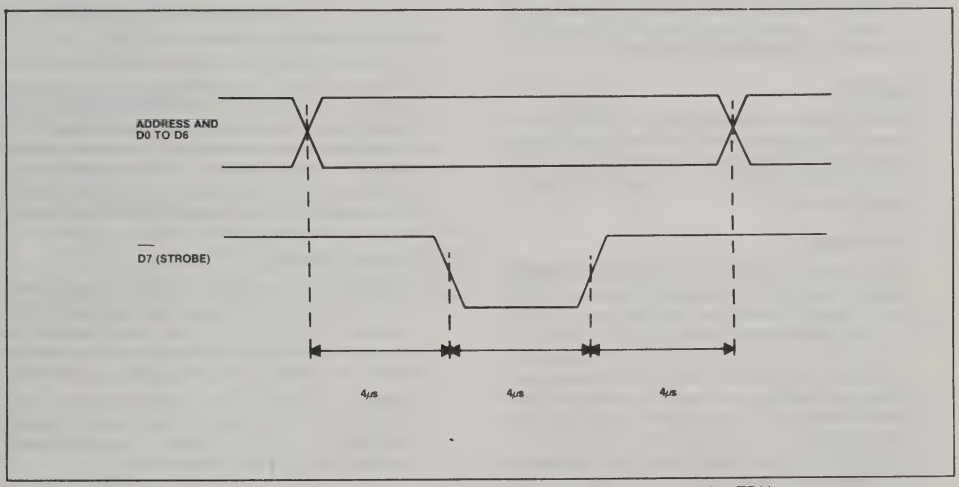


Fig. 2 Typical timing diagram for input data strobing of control data using TS11

DISPLAY OPTIONS

Logic is contained on the Video Generator chip to process the Display Modes as described in the Broadcast Teletext Specification. These facilities are outlined below. Some extra facilities are also included.

1. **Character Set**

   The chip can display 96 Alphanumerics characters and 64 Graphics shapes which may be either contiguous or separated. The alphanumeric format is determined by a 4320 bit Read Only Memory organised as:

   96 (characters) x 5 (dots) x 9 (lines) = 4320

   This can be programmed for different character fonts.

   The graphics shapes are determined directly from the bits of the character code (Fig.10).

2. **Display and Background Colour**

   The characters and the background can be displayed in one of seven colours. In addition the background may be black. This information is stored in two sets of three latches representing character and background colours.

3. **Conceal and Flash**

   Selected characters can be concealed and optionally revealed by the viewer. Selected characters can be flashed on command. The flashing is controlled by an on-chip flash oscillator. During the flash period or when concealed, only background information is displayed. The flash rate is 1.56Hz.

4. **Boxing**

   Text or graphics characters can be boxed into a normal video picture. While in Picture mode boxing is automatic if Newsflash or Sub-title (and Sss = Ddd). Other boxed characters may be manually revealed by Reveal command.

5. **Double Height**

   Double height characters are characters contained between the control characters "Double Height" and "Normal Height" (or end of line). When a "Double Height" control character is read from the RAM only the top half of the subsequent character(s) are displayed during the 10 raster scans. During the next 10 scan lines, 40 is subtracted from the addresses being output on A0–A9 so the same 40 addresses are read from another 10 times. Characters which are not double height are displayed as the background colour and the bottom(s) of the double height character(s) is (are) displayed.

6. **Hold Graphics**

   When this latch is set, any subsequent control characters (except change Double/Normal Height or Change Alpha/Graphics) are displayed as the last graphics character.

7. **Special Graphics**

   While in Graphics Mode the Special Graphics command will give a special high resolution facility. In this mode there is a one to one correspondence between data bits b_1, b_2, b_3, b_4, b_5, b_7 and the six dots in each horizontal line of a character. This gives a possible graphics resolution of 6 x 20 for each character in interlace mode (or 6 x 10 if not interlaced).

8. **Box Clock**

   When box clock is selected in picture mode and teletext the last eight characters of the page header are boxed in double height. To ensure that the "live" clock is displayed the store address is temporarily switched to that defined by Sss. This function is cleared in text mode.

9. **Box Header**

   When box header is selected in picture mode and teletext the page header is boxed in double height (not if bottom half of page selected).

10. **Half-page Operation**

    This allows either the top or bottom half of a normal Teletext/Viewdata page to be displayed over the whole screen, with each character in double height. This makes the display easier to read from a distance. Double height characters are ignored in this mode.

11. **Monochrome Output/Mix Mode**

    In normal operation the Picture/$\overline{\text{Text}}$ Output is used to blank the normal picture information for boxing or displaying a page of text.

    In the mix mode this outputs Monochrome text information which is matched to the Gun Output signals in delay and drive. This can be used to superimpose text onto a picture by "cutting away" the picture below text data or as an output for Monochrome displays or printers. In this mode coloured backgrounds are suppressed for viewing clarity. The output is at a low level to display a character.

12. **Character Rounding**

    Characters are normally rounded by adding half dots to smooth diagonals. For normal height characters the extra TV lines made available by interlace are utilised for this and so if in non-interlace mode single height characters cannot be rounded.

    Character rounding can be inhibited totally by a signal from Control and in this mode, intended specifically for printers, flashing is also suppressed. Reset by P key or new Viewdata page.

13. **Cursor**

    The cursor is stored as the 8th bit of the appropriate character in the Data Store. When switched on it is displayed as a bar on the bottom line of the character rectangle flashing between foreground colour and black in anti-phase to normal flashing characters.

14. Non Interlaced Operation

When interlaced composite sync. is input to the chip it operates in normal Interlaced Mode and regenerates Interlaced composite sync.

If there is no incoming sync. the chip switches to the OFF hours mode.

If the Phase Comparator output is pulled high, e.g. 4k7 to Vcc, Interlaced Sync. is output. If the Phase Comparator output is held low Non Interlaced Sync. is output and character rounding for single height characters is inhibited.

SIGNAL DETECTION CRITERIA (For On Hours Operation)

The Video Generator detection circuitry for incoming sync. signals is designed to prevent mis-operation in the presence of noise. The criteria for detection is defined below.

1. Line Sync

The Comp. Video Input must be negative for greater than 3μs.

2. Frame Sync.

The Comp. Video Input must be negative for greater than 12μs and at least 310 lines (Line Flyback pulses) must have occurred since the previous Frame Sync detection.

3. Odd Frame Detection

Odd Frame Detection occurs when a Line Flyback pulse falls in a window 12–39μs after Frame Sync Detection. This is used to lock the line counter.

4. On-Hours/Off-Hours Detection

The incoming line flyback and line sync pulses are compared to determine whether a valid transmission is being received. Lack of coincidences/frame are accumulated and if more than 16/Frame occur for a period 350–1000ms the logic deems that a valid transmission is not being received and the chip switches 'OFF Hours''. If however, less than eight occur in any two successive ½ frames, the logic deems that a valid Composite Sync is being received and the system goes 'ON Hours'.

For the chip to be able to look for synchronism the following phase relationship between Line Flyback and Comp. Sync must be satisfied.

(a) Earliest back edge of LFB is 2μs after leading edge of line sync.

(b) Latest leading edge of LFB is 2μs after leading edge of line sync.

(c) Latest back edge of LFB is 12μs after leading edge of line sync.

The minimum length of the LFB pulse is 8μs.

5. 6MHz Display Oscillator

The 6MHz display oscillator must run fast in the OFF Hours mode but not so fast that the ON/OFF Hours detection criteria cannot be satisfied. This sets a maximum offset of +1.5kHz, the minimum offset is set by lock time criteria and would typically be +0.5kHz.

The frequency range of the oscillator must extend below the 6.0MHz nominal frequency. The minimum frequency should be at least −0.5kHz but can be as low as convenient.

COMPOSITE SYNC INPUT

On chip D.C. restore is provided which allows simple interfacing to the television, either composite sync. signals or video being acceptable.

As the Composite Sync/Video signal from the television may not be referenced to the system earth it is a.c. coupled to the chip.

A typical Interface Circuit is shown in Fig.3.

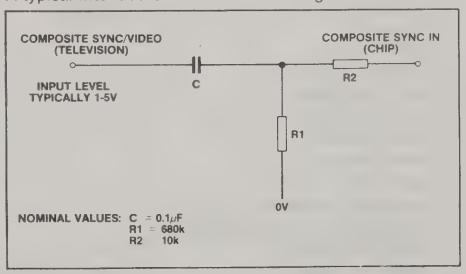


Fig.3 Typical interface circuit

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to Vss . . . . . –0.3 to +15V
Storage temperature range. . . . . –55°C to +150°C

*Exceeding these ratings could cause permanent damage
Functional operation is not guaranteed under these conditions
Operating ranges are specified below

Standard Conditions (unless otherwise indicated)

Vss = OV (Substrate voltage)
Vcc = +5V ±5%
Vdd = +12V ±10%
Operating Temperature (Ta) = 0°C to +70°C

Clock Frequency 6.0MHz

Characteristic	Min	Typ**	Max	Units	Conditions
INPUTS					
Chip Select					
Input Logic High	2.4		Vcc	V	
Input Logic Low	Vss		0.8	V	
Input Current	10	25	100	μA	Vin = 5V
Comp. Sync.					
Input Logic High	1.0		Vcc	V	
Input Logic Low	–0.3		0.05	V	See Note 1
Input Capacitance			15	pF	Vin = 0V
Source Current		50		μA	Vin = 0V
6MHz					
Input Logic High	2.8		Vdd	V	
Input Logic Low	Vss		0.4	V	
Input Capacitance			25	pF	Vin = 0V
Mark to Space Ratio	40:60		60:40		
Frequency	1.0		6.5	MHz	
Input Leakage			10	μA	Vin = 12V
All Other Inputs					
Input Logic High	2.4		Vdd	V	
Input Logic Low	Vss		0.8	V	
Input Capacitance			15	pF	Vin = 0V
Input Leakage			10	μA	Vin = 12V
OUTPUTS					
Addresses, Read/$\overline{\text{Write}}$					
Store Select (Tri-State) (Note 2)					
Logic High Output	2.4		Vcc	V	Ioh = -300μA
Logic Low Output	Vss	0.2	0.5	V	Iol = 3.0mA
Capacitance			15	pF	Vin = 0V
T rise T fall			200	ns	C load = 200pF
Leakage (Disabled)			10	μA	Vo = 0V, 5V
Time Slots (TS1, TS2)					
(Push-Pull)					
Logic High Output	2.4		Vcc	V	Ioh = -300μA
Logic Low Output	Vss	0.2	0.5	V	Iol = 3.0mA
T rise T fall			200	ns	C load = 200pF
Comp. Sync (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 1.6mA
Logic High Leakage			10	μA	Vo = 12V
Capacitance			20	pF	Vo = 0V
Delay from Comp. Sync In.			1	μs	ON Hours only

Characteristic	Min	Typ**	Max	Units	Conditions
$\overline{\text{RSYNC}}$ (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 4.0mA
Logic High Leakage			10	μA	Vo = 5V
Capacitance			15	pF	Vo = 0V
Phase Comparator (Open Drain)					
Logic Low Output	Vss		0.5	V	Iol = 4.0 mA
Logic High Leakage			10	μA	Vo = 12V
Capacitance			15	pF	Vo = 0V
R.G.B. Outputs Picture/Text Output (Tristate) (Note 2)					
Logic High Output	Vcc−1		Vcc	V	I source = 1mA
Logic Low Output	Vss		1	V	I sink. = 2mA
Capacitance			20	pF	Vin = 0V
T rise T fall (10%–90%)			30	ns	CL = 30pF
Differential T rise T fall			30	ns	CL = 30pF Note 3
19.2kHz, 1.2kHz Outputs					
Logic High Output	2.4		Vcc	V	Ioh = -30μA.
Logic Low Output	Vss	0.2	0.5	V	Iol = 300μA
T rise T fall			1	μs	C load = 100pF
POWER					
Vcc Supply		25	40	mA	Vcc = 5V
Vdd Supply		50	80	mA	Vdd = 12V

Note 1: Voltages below −0.3 volts should be current limited to 1mA.

Note 2: All tristated when $\overline{\text{Chip Select}}$ = Vcc. R.G.B. outputs also tristated when displaying picture and not mixed.

Note 3: Picture/$\overline{\text{Text}}$ matched in mix mode only.

** Typical values are at +25°C and nominal voltages.

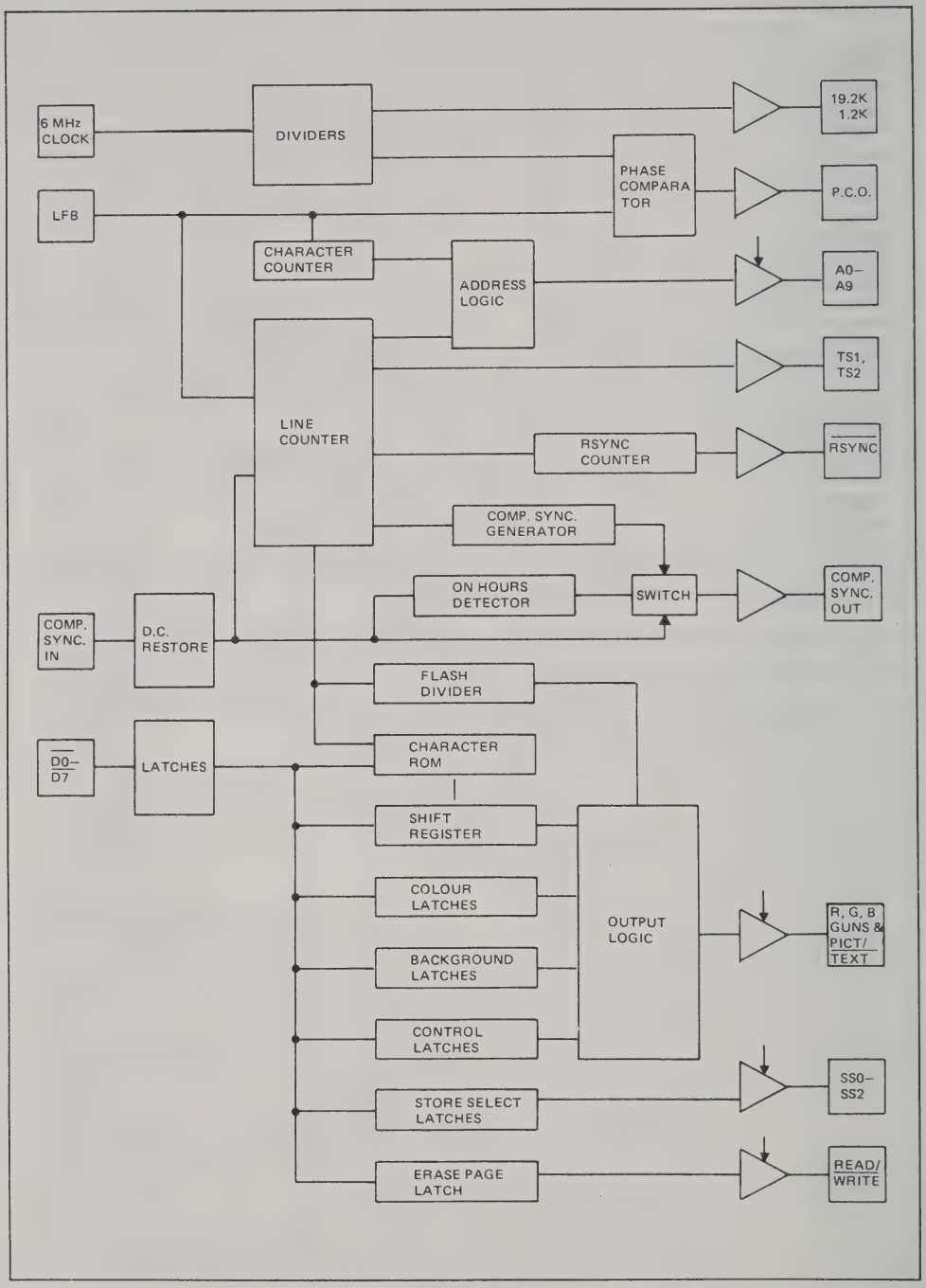


Fig.4 Block diagram

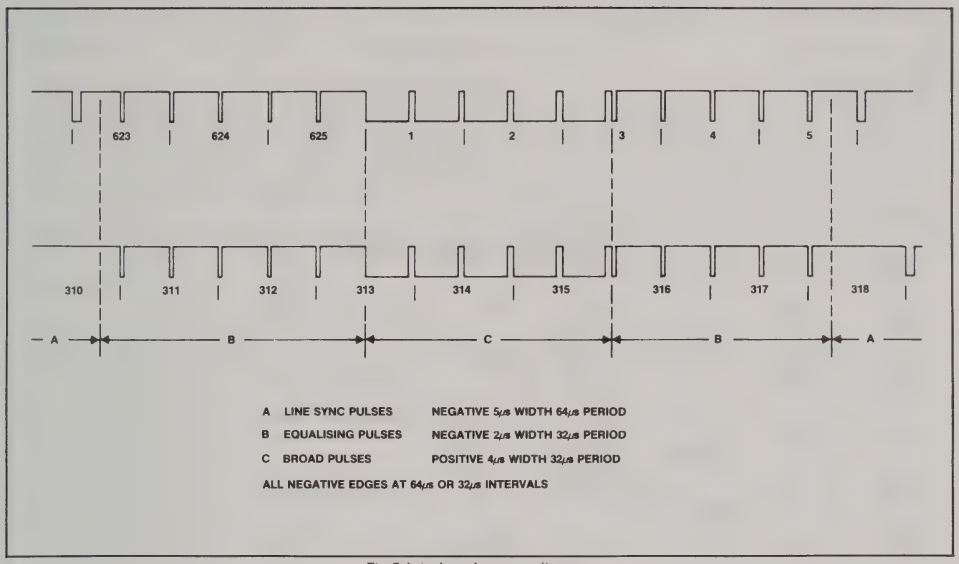


Fig.5 Interlaced composite sync

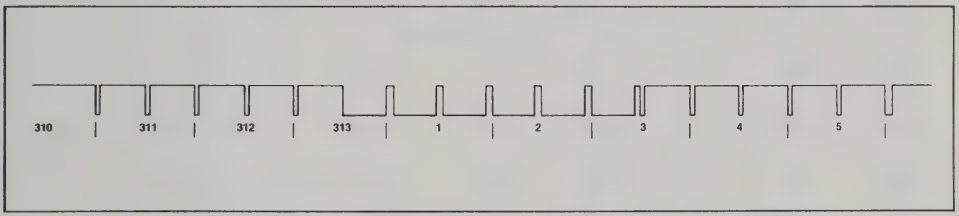


Fig.6 Non interlaced composite sync output

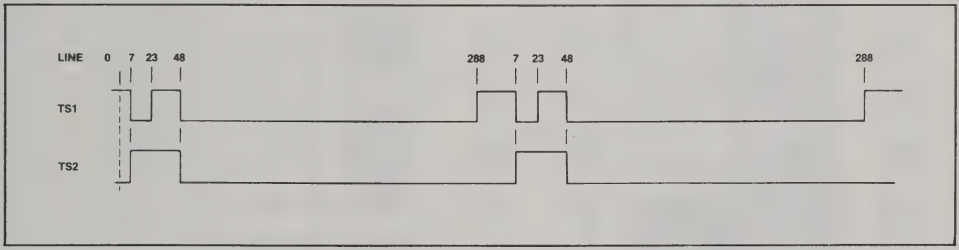


Fig.7 Time slot outputs non interlaced

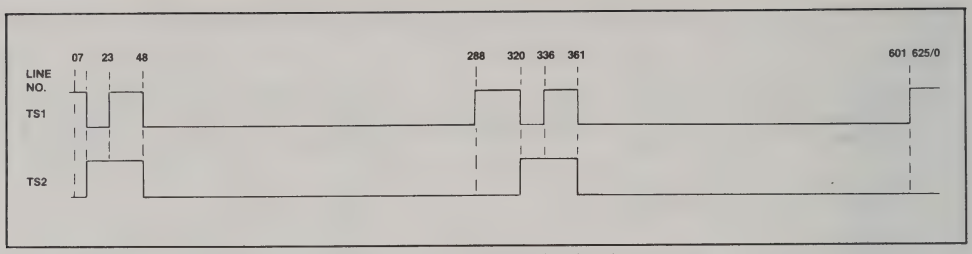


Fig.8 Time slot outputs (interlaced)

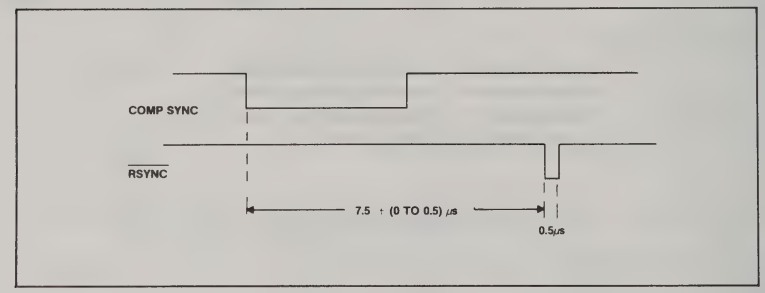


Fig.9 RSYNC timing

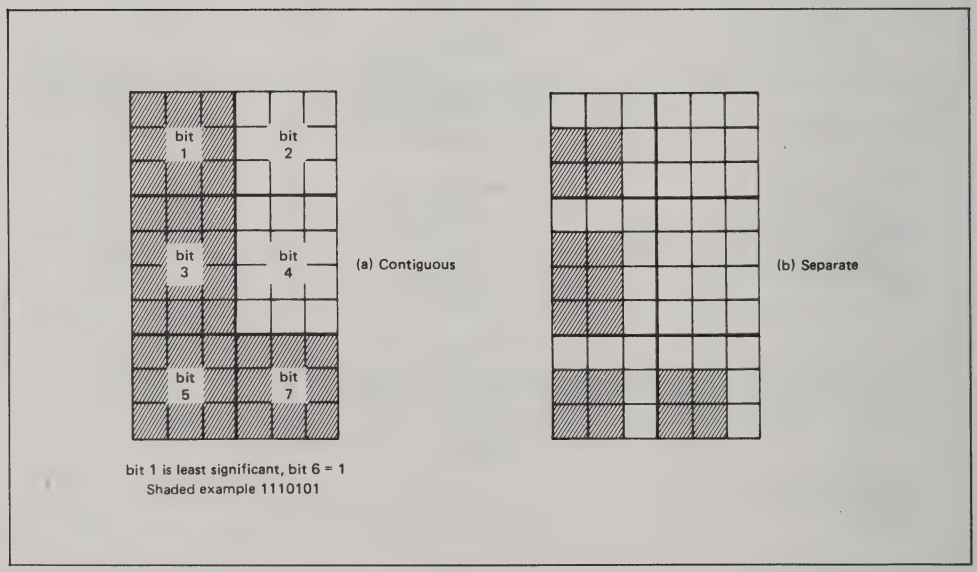


Fig.10 Graphics format

b7 b6 b5 / Bits b4 b3 b2 b1 / Col / Row	0_{0_0}	0_{0_1}	0_{1_0}		0_{1_1}		1_{0_0}	1_{0_1}	1_{1_0}		1_{1_1}	
0 0 0 0 / 0	NUL①	DLE①			O		@	P	–		p	
0 0 0 1 / 1	Alpha^{n} Red	Graphics Red	!		1		A	Q	a		q	
0 0 1 0 / 2	Alpha^{n} Green	Graphics Green	"		2		B	R	b		r	
0 0 1 1 / 3	Alpha^{n} Yellow	Graphics Yellow	£		3		C	S	c		s	
0 1 0 0 / 4	Alpha^{n} Blue	Graphics Blue	$		4		D	T	d		t	
0 1 0 1 / 5	Alpha^{n} Magenta	Graphics Magenta	%		5		E	U	e		u	
0 1 1 0 / 6	Alpha^{n} Cyan	Graphics Cyan	&		6		F	V	f		v	
0 1 1 1 / 7	Alpha^{n}② White	Graphics White	'		7		G	W	g		w	
1 0 0 0 / 8	Flash	Conceal Display	(		8		H	X	h		x	
1 0 0 1 / 9	Steady②	Contiguous② Graphics	)		9		I	Y	i		y	
1 0 1 0 / 10	End Box②	Separated Graphics	*		:		J	Z	j		z	
1 0 1 1 / 11	Start Box	ESC①	+		;		K	←	k		¼	
1 1 0 0 / 12	Normal Height②	Black② Background	,		<		L	½	l		II	
1 1 0 1 / 13	Double Height	New Background	-		=		M	→	m		¾	
1 1 1 0 / 14	Special Graphics	Hold Graphics	.		>		N	↑	n		÷	
1 1 1 1 / 15	Normal② Graphics	Release② Graphics	/		?		O	=	o		■	

① These control characters are reserved for compatibility with other data codes

② These control characters are presumed before each row begins

Codes may be referred to by their column and row e.g. 2/5 refers to %

Character rectangle

Black represents display colour

White represents background

Fig.11 Teletext character codes (002 character set)

PLESSEY
Semiconductors

MS1002

851 ELEMENT CCD ANALOGUE STORE

The Plessey MS1002 is a clock controlled analogue shift register for applications including time delay, compression/expansion and temporary storage of analogue or digital signals. Information is transferred through the device by two externally supplied clocks; the timing between the clocks is not critical. A soft line clamp facility is available so that the input can be referenced to a desired voltage level. Internal thermal compensation circuits correct for any drift in CCD bias over a wide range of temperature.

The device is available in two grades as follows:

MS1002-1 selected for analogue storage with interrupted clocks.

MS1002-3 selected for delay line operation with continuous clocks.

FEATURES

- Typically 5MHz Video Bandwidth With A Clock Frequency of 13.3MHz
- 15V Supply Operation
- Internal Thermal Compensation To Correct For Any Drifts in CCD Input Bias
- Soft Line Clamp Facility

APPLICATIONS

- Electrically Variable Analogue Delay
- Line Store: Full PAL TV Line Can Be Stored With A Clock Frequency (13.3MHz) Of Three Times The Colour Subcarrier Frequency
- Time Base Correction
- Time Compression/Expansion

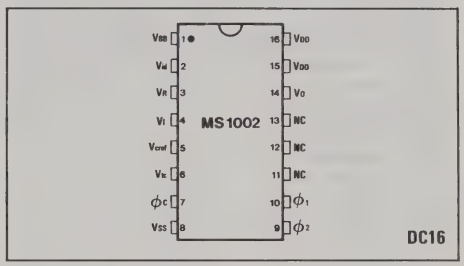


Fig.1 Pin connections - top view

PIN NAMES

V_{BB}	Substrate Bias
V_{id}	Internal Diode Bias
V_R	Reference Input
V_I	Analogue Input
V_{cref}	Clamp Reference Bias
V_{tc}	Thermal Compensation Bias
Φ_C	Clamp Pulse
V_{DD}	Drain Supply
V_O	Analogue Output
NC	Not Connected
Φ_1	Clock 1
Φ_2	Clock 2
V_{SS}	Ground

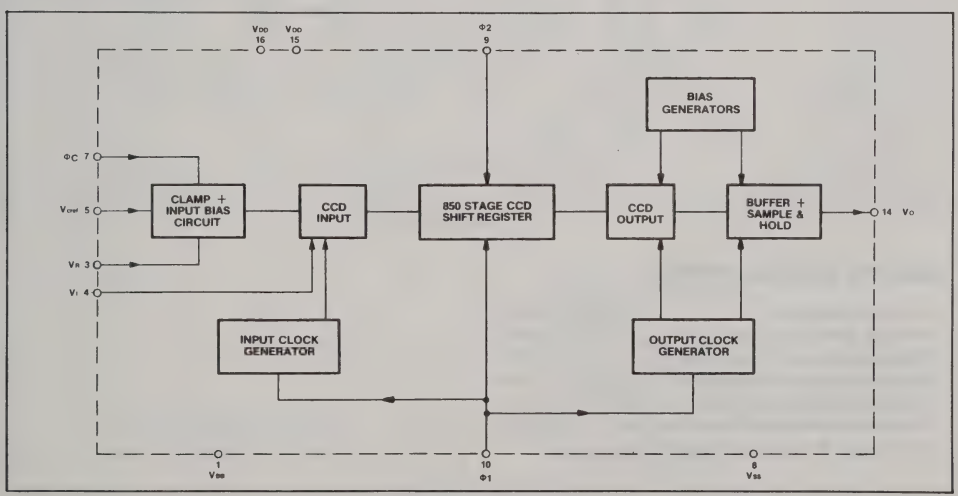


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{BIAS} = 4V, $\Phi_C = \Phi_{CL}$, V_{DD} = 15V, V_{BB} = -5V, Φ_L = 0.8V, Φ_H = 12.5V, fΦ = 13.3MHz, f_{sig} = 1kHz, T = 25°C

Characteristic	Symbol	Value			Units	Notes
		Min.	Typ.	Max.		
Supply current	I_{DD}		12	16	mA	$\Phi_1 = \Phi_H, \Phi_2 = \Phi_L$
Substrate current	I_{BB}		10	20	μA	
Gain	G	-2	0	+2	dB	V_{in} = 100mV pk/pk
Differential gain	ΔG			3	%	V_{in} = 1V pk/pk
Bandwidth	BW	4.5	5		MHz	V_{in} = 1V pk/pk
Random noise	RN			0.8	mV	Bandwidth = 4.5MHz
Spatial noise (1)	SN			2.5	mV	Hold time = 1ms $\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Rate of output signal offset (1)	RSO			3	mV/ms	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Output droop rate (1)	V_O/T		4	8	V/s	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Signal input leakage	I_{in}		0.1		nA	
Signal input capacitance	C_{in}		4	7	pF	
Output resistance	R_O		0.4	1	kΩ	
Clock capacitance						
Phase/phase Φ_1/Φ_2	CΦ^1		75	100	pF	
Phase/gnd	CΦ		60	80	pF	Φ_1 and Φ_2
Clamp capacitance	$C_{\Phi C}$	2		7	pF	
T = +70°C						
Spatial noise (1)	SN			50	mV	Hold time = 1ms $\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Rate of output signal offset (1)	RSO			70	mV/ms	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Output droop rate (1)	V_O/T			200	V/S	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Signal input leakage	I_{in}			100	nA	

NOTE
(1) applies to MS1002-1 only

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Value		Units	Notes
		Min.	Max.		
Supply voltage - positive	V_{DD}	14.5	15.5	V	
Substrate bias supply	V_{BB}	-6	-4	V	
Clock low	Φ_L	-1	0.8	V	All clock inputs
Clock high	Φ_H	12.5	V_{DD}	V	All clock inputs
Clamp low	Φ_{OL}	-1	0.8	V	
Clamp high	Φ_{CH}	11.0	V_{DD}	V	
Input bias range	V_{BIAS}	3.5	4.5	V	V_{in} = 100mV pk/pk
Clock frequency	fΦ	-	25	MHz	
Output load					
Resistance	R_L	10	-	kΩ	
Capacitance	C_L	-	15	pF	
Ambient operating temperature	T	0	70	°C	

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-65°C to +100°C
Ambient operating temperature	0°C to +70°C
Max.positive supply voltage (V_{DD})	+19V
Min.negative supply voltage (V_{BB})	-6V
Max.voltage on any pin (except V_{DD} , V_{BB})	V_{DD}
Min.voltage on any pin (except V_{DD} , V_{BB})	V_{BB} -0.3V
All voltages with respect to V_{SS} (Ground)	

PRECAUTIONS

This device has limited immunity to static electricity when handled. The conductive foam or plastic carrier provided should be retained until the device is incorporated in its circuit. Any handling of the device without its plastic carrier should be minimised. Care should be taken to avoid any static discharges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

Care should also be taken to avoid voltage transients in the supply leads. These can occur when the supplies are switched on or off. The track length from the clock drivers to the CCD store should be minimised to prevent overshoots on the clock waveforms. It is permissible to allow these overshoots to exceed the minimum and maximum clock voltage specifications by up to 2V for not longer than 10ns duration per clock transition.

GENERAL OPERATION

The circuit operates as a sampled shift register under the control of the external clocks Φ_1 and Φ_2. Analogue input signals are sampled on the falling edge of the Φ_1 clock and are subsequently stored and shifted through the device to appear at the output after 850 complete clock cycles (see timing diagram in Fig.3 for exact delay information). Each output sample is presented on the falling edge of Φ_1 and exists for an entire clock period. The output waveform consists of the delayed and/or stored analogue information plus components of the inverse Φ_1 clock due to breakthrough from internal sample and hold circuits. Connections for two-phase operation are shown in Fig.4. If the soft line clamp facility is not desired, it may be disabled by connecting Φ_C to V_{SS}. In this case, to maintain correct input biassing, the wiper of R_V should be connected to pin 4 instead, via a resistor, as shown in Fig.5. The device exhibits signal inversion.

Delay mode

Incoming signals are applied to the terminal V_I via a coupling capacitor (Fig.4).The injected signal is proportional to the difference between V_I and V_R. It is necessary for the user to ensure that the incoming analogue signal contains no frequency components in excess of $f\Phi \div 2$ in order to avoid spurious components, due to aliassing, appearing at the output. The output waveform is available directly from the device, or may be taken via a suitable buffer circuit if a lower output impedance is required. Analogue information appears at the output terminal delayed in time by 851 clock cycles. The frequency response characteristics of the device are related to the clock frequency, $f\Phi$ as shown in Fig.6.

The clock frequency is variable over a wide range. At high frequencies ($>$ 25MHz) the bandwidth of the device becomes limited owing to the decreasing efficiency of the charge coupled shift register. At low frequencies ($<$ 100kHz) the signal range is diminished because of the generation of thermal charge in the shift register; hence the minimum clock frequency is related to the maximum operating temperature (the 100kHz figure corresponding to 70°C operation). The device should be located away from circuit components which dissipate power and should be provided with the coolest ambient offered by the system. Heat dissipation from the analogue store itself may be assisted by soldering uncommitted pins to an earth plane. At low frequencies the effects of thermally generated currents can be minimised by using clocks having a short Φ_1 on-duration ($t_4 \approx$ 100ns). This approach also simplies the filtering of clock noise from the output. A 100nF decoupling capacitor on pin 6 may be necessary in some applications.

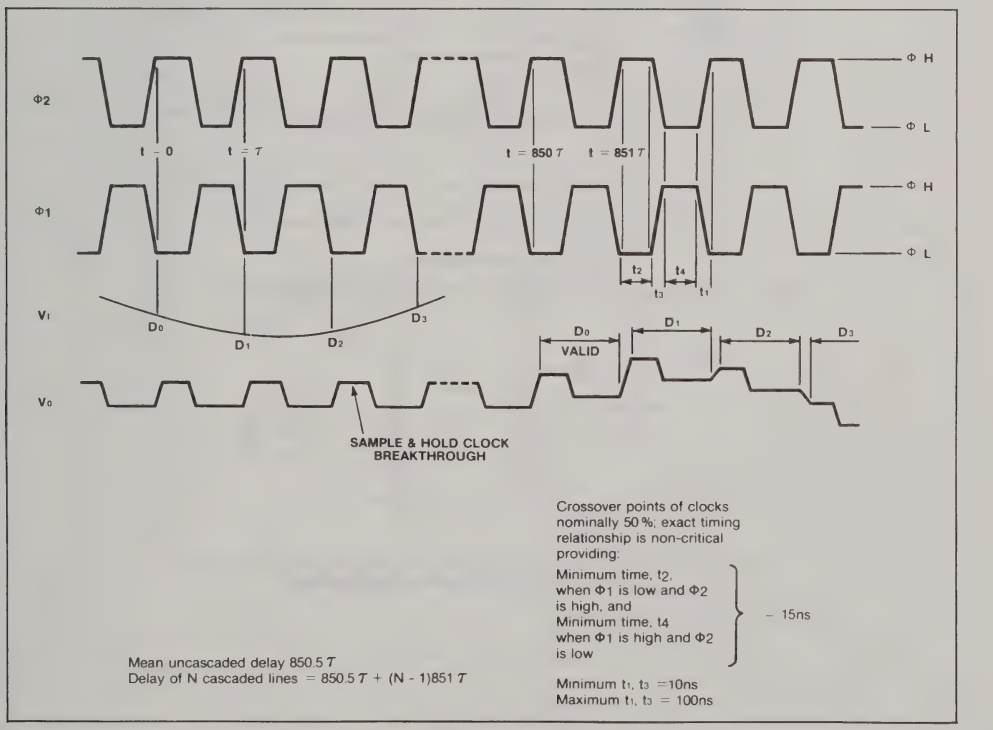


Fig.3 Timing diagram

Time compression/expansion

Compression or expansion of analogue signals in the time domain may be achieved by loading and unloading the shift register at different frequencies. The low frequency limit for this mode of operation is dictated by the rate of average signal offset (RSO) as this will reduce the maximum output signal amplitude.

Analogue storage

When the shift register has been loaded with analogue signals, the clocks may be interrupted to achieve temporary storage of the information. The samples are retrieved when the clocks are subsequently re-started. The clocks must be stopped in the state $\Phi_1 = \Phi_L$ in order to minimise degradation of the signal due to thermal leakage currents. The maximum hold time is determined by the spatial noise parameter (SN). Spatial noise magnitude is a function of stop clock period and of operating temperature as shown in Fig.7. MS1002-1 devices are tested in the stopped clock mode and spatial noise parameters guaranteed for this type of operation.

Component values

C_O	Output Capacitor, 1.0μF
C_I	Input Capacitor, 0.1μF
R_I	Input Resistor, 47kΩ
R_V	Variable Resistor, 200kΩ
R_f	Fixed Resistor, 820kΩ
R_L	Load Resistor, 10kΩ (including measuring
C_L	Load Capacitor, 15pF kit impedance)
C_D	Decoupling Capacitors, 10nF

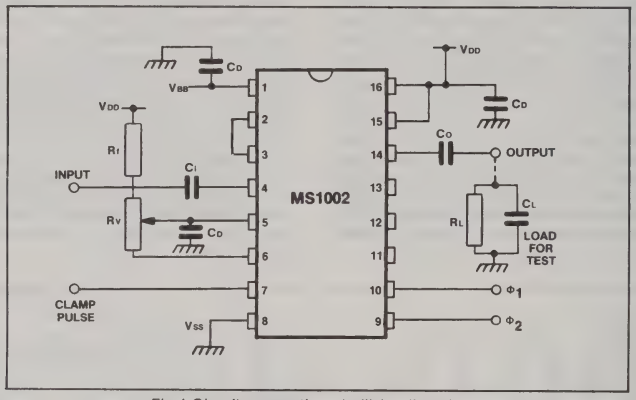


Fig.4 Circuit connections (utilising line clamp)

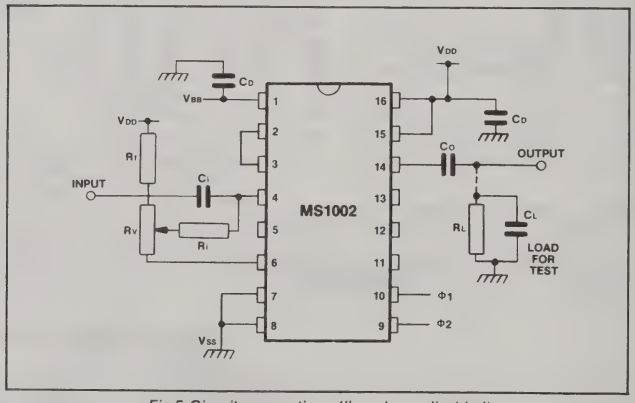


Fig.5 Circuit connections (line clamp disabled)

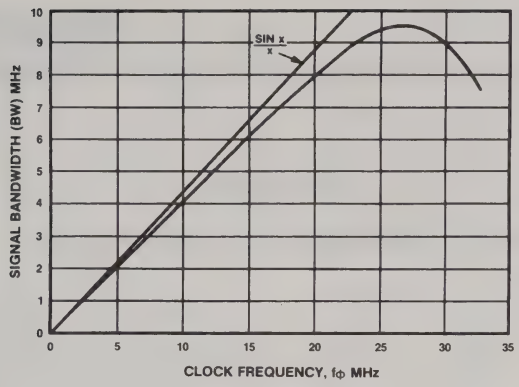


Fig.6 Typical bandwidth

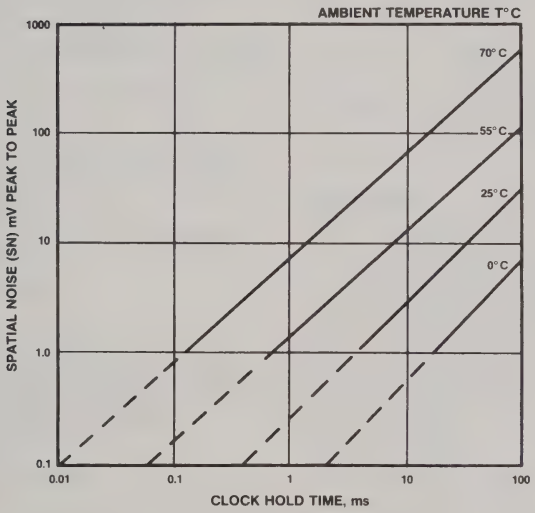


Fig.7 Typical output spatial noise as a function of clock hold time and operating temperature

PLESSEY
Semiconductors

MS1003

910 ELEMENT CCD ANALOGUE STORE

The Plessey MS1003 is a clock controlled analogue shift register for applications including time delay, compression/expansion and temporary storage of analogue or digital signals. Information is transferred through the device by two externally supplied clocks; the timing between the clocks is not critical. A soft line clamp facility is available so that the input can be referenced to a desired voltage level. Internal thermal compensation circuits correct for any drift in CCD bias over a wide range of temperature.

The device is available in two grades as follows:

MS1003-1 selected for analogue storage with interrupted clocks.

MS1003-3 selected for delay line operation with continuous clocks.

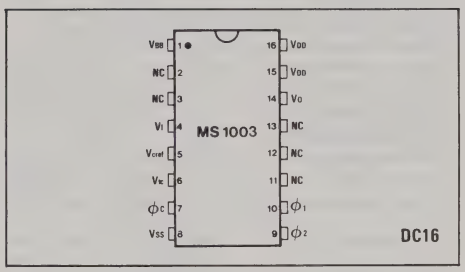


Fig.1 Pin connections - top view

FEATURES

- Typically 5MHz Video Bandwidth With A Clock Frequency of 14.3MHz
- 15V Supply Operation
- Internal Thermal Compensation To Correct For Any Drifts in CCD Input Bias
- Soft Line Clamp Facility

APPLICATIONS

- Electrically Variable Analogue Delay
- Line Store: Full NTSC TV Line Can Be Stored With A Clock Frequency (14.3MHz) Of Four Times The Colour Subcarrier Frequency
- Time Base Correction
- Time Compression/Expansion

PIN NAMES

V_{BB}	Substrate Bias
V_I	Analogue Input
V_{cref}	Clamp Reference Bias
V_{TC}	Thermal Compensation Bias
Φ_C	Clamp Pulse
V_{DD}	Drain Supply
V_O	Analogue Output
NC	Not Connected
Φ_1	Clock 1
Φ_2	Clock 2
V_{SS}	Ground

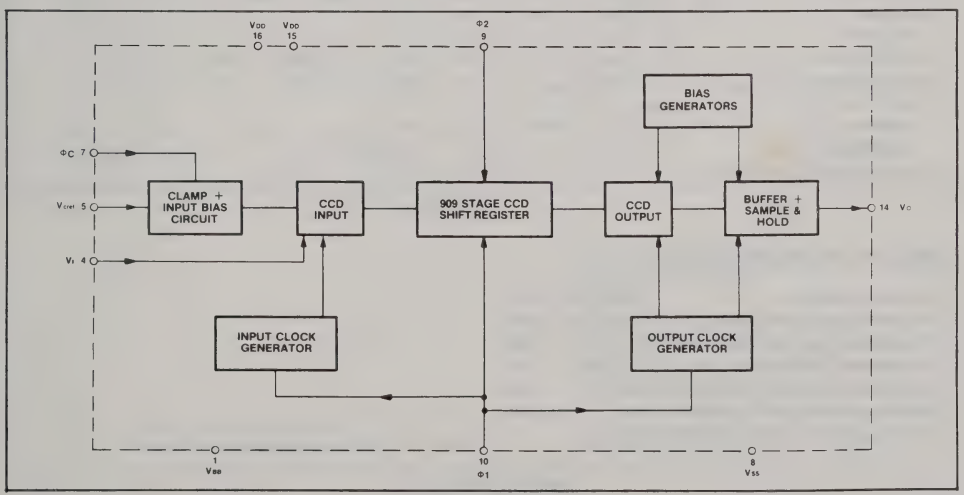


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{BIAS} = 4V, $\Phi_C = \Phi_{CL}$, V_{DD} = 15V, V_{BB} = -5V, Φ_L = 0.8V, Φ_H = 12.5V, fΦ = 14.3MHz, f_{sig} = 1kHz, T = 25°C

Characteristic	Symbol	Value			Units	Notes
		Min.	Typ.	Max.		
Supply current	I_{DD}		12	16	mA	$\Phi_1 = \Phi_H, \Phi_2 = \Phi_L$
Substrate current	I_{BB}		10	20	μA	
Gain	G	-2	0	+2	dB	V_{in} = 100mV pk/pk
Differential gain	ΔG			3	%	V_{in} = 1V pk/pk
Bandwidth	BW	4.5	5		MHz	V_{in} = 1V pk/pk
Random noise	RN			0.8	mV	Bandwidth = 4.5MHz
Spatial noise (1)	SN			2.5	mV	Hold time = 1ms $\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Rate of output signal offset (1)	RSO			3	mV/ms	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Output droop rate (1)	V_O/T		4	8	V/s	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Signal input leakage	I_{in}		0.1		nA	
Signal input capacitance	C_{in}		4	7	pF	
Output resistance	R_O		0.4	1	kΩ	
Clock capacitance						
Phase/phase Φ_1/Φ_2	$C\Phi_1$		80	110	pF	
Phase/gnd	CΦ		65	86	pF	Φ_1 and Φ_2
Clamp capacitance	$C_{\Phi C}$	2		7	pF	
T = +70°C						
Spatial noise (1)	SN			50	mV	Hold time = 1ms $\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Rate of output signal offset (1)	RSO			70	mV/ms	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Output droop rate (1)	V_O/T			200	V/S	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Signal input leakage	I_{in}			100	nA	

NOTE
(1) applies to MS1003-1 only

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Value		Units	Notes
		Min.	Max.		
Supply voltage - positive	V_{DD}	14.5	15.5	V	
Substrate bias supply	V_{BB}	-6	-4	V	
Clock low	Φ_L	-1	0.8	V	All clock inputs
Clock high	Φ_H	12.5	V_{DD}	V	All clock inputs
Clamp low	Φ_{OL}	-1	-0.8	V	
Clamp high	Φ_{CH}	11.0	V_{DD}	V	
Input bias range	V_{BIAS}	3.5	4.5	V	V_{in} = 100mV pk/pk
Clock frequency	fΦ	-	25	MHz	
Output load					
Resistance	R_L	10	-	kΩ	
Capacitance	C_L	-	15	pF	
Ambient operating temperature	T	0	70	°C	

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-65°C to +100°C
Ambient operating temperature	0°C to +70°C
Max.positive supply voltage (V_{DD})	+19V
Min.negative supply voltage (V_{BB})	-6V
Max.voltage on any pin (except V_{DD}, V_{BB})	V_{DD}
Min.voltage on any pin (except V_{DD}, V_{BB})	V_{BB} -0.3V
All voltages with respect to V_{SS} (Ground)	

PRECAUTIONS

This device has limited immunity to static electricity when handled. The conductive foam or plastic carrier provided should be retained until the device is incorporated in its circuit. Any handling of the device without its plastic carrier should be minimised. Care should be taken to avoid any static discharges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

Care should also be taken to avoid voltage transients in the supply leads. These can occur when the supplies are switched on or off. The track length from the clock drivers to the CCD store should be minimised to prevent overshoots on the clock waveforms. It is permissible to allow these overshoots to exceed the minimum and maximum clock voltage specifications by up to 2V for not longer than 10ns duration per clock transition.

GENERAL OPERATION

The circuit operates as a sampled shift register under the control of the external clocks Φ_1 and Φ_2. Analogue input signals are sampled on the falling edge of the Φ_1 clock and are subsequently stored and shifted through the device to appear at the output after 909 complete clock cycles (see timing diagram in Fig.3 for exact delay information). Each output sample is presented on the falling edge of Φ_1 and exists for an entire clock period. The output waveform consists of the delayed and/or stored analogue information plus components of the inverse Φ_1 clock due to breakthrough from internal sample and hold circuits. Connections for two-phase operation are shown in Fig.4. If the soft line clamp facility is not desired, it may be disabled by connecting Φ_C to Vss. In this case, to maintain correct input biassing, the wiper of Rv should be connected to pin 4 instead, via a resistor, as shown in Fig.5. The device exhibits signal inversion.

Delay mode

Incoming signals are applied to the terminal V_I via a coupling capacitor (Fig.4). It is necessary for the user to ensure that the incoming analogue signal contains no frequency components in excess of $f\Phi \div 2$ in order to avoid spurious components, due to aliassing, appearing at the output. The output waveform is available directly from the device, or may be taken via a suitable buffer circuit if a lower output impedance is required. Analogue information appears at the output terminal delayed in time by 910 clock cycles. The frequency response characteristics of the device are related to the clock frequency, $f\Phi$ as shown in Fig.6.

The clock frequency is variable over a wide range. At high frequencies ($>$ 25MHz) the bandwidth of the device becomes limited owing to the decreasing efficiency of the charge coupled shift register. At low frequencies ($<$ 100kHz) the signal range is diminished because of the generation of thermal charge in the shift register; hence the minimum clock frequency is related to the maximum operating temperature (the 100kHz figure corresponding to 70°C operation). The device should be located away from circuit components which dissipate power and should be provided with the coolest ambient offered by the system. Heat dissipation from the analogue store itself may be assisted by soldering uncommitted pins to an earth plane. At low frequencies the effects of thermally generated currents can be minimised by using clocks having a short Φ_1 on-duration ($t_4 \approx$ 100ns). This approach also simplifies the filtering of clock noise from the output. A 100nF decoupling capacitor on pin 6 may be necessary in some applications.

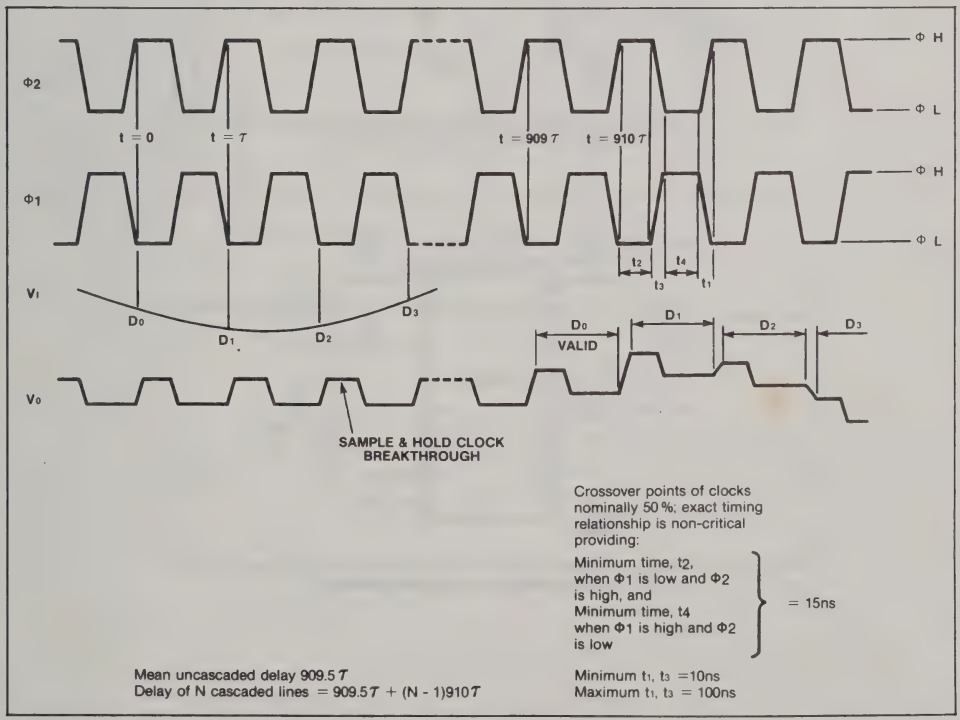


Fig.3 Timing diagram

Time compression/expansion

Compression or expansion of analogue signals in the time domain may be achieved by loading and unloading the shift register at different frequencies. The low frequency limit for this mode of operation is dictated by the rate of average signal offset (RSO) as this will reduce the maximum output signal amplitude.

Analogue storage

When the shift register has been loaded with analogue signals, the clocks may be interrupted to achieve temporary storage of the information. The samples are retrieved when the clocks are subsequently re-started. The clocks must be stopped in the state $\Phi_1 = \Phi_L$ in order to minimise degradation of the signal due to thermal leakage currents. The maximum hold time is determined by the spatial noise parameter (SN). Spatial noise magnitude is a function of stop clock period and of operating temperature as shown in Fig.7. MS1003-1 devices are tested in the stopped clock mode and spatial noise parameters guaranteed for this type of operation.

Component values

C_O	Output Capacitor, 1.0μF
C_i	Input Capacitor, 0.1μF
R_i	Input Resistor, 47kΩ
R_V	Variable Resistor, 200kΩ
R_f	Fixed Resistor, 820kΩ
R_L	Load Resistor, 10kΩ (including measuring
C_L	Load Capacitor, 15pF kit impedance)
C_D	Decoupling Capacitors, 10nF

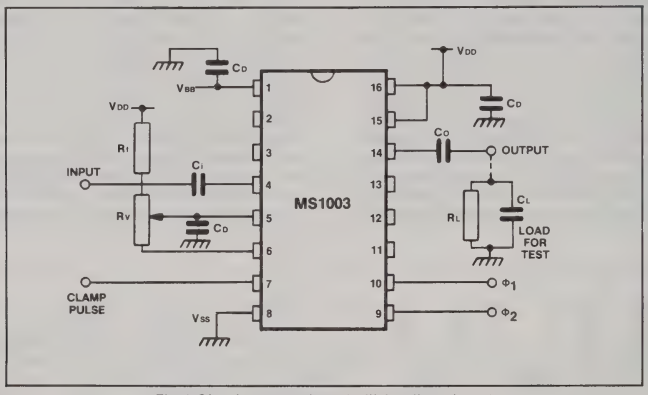


Fig.4 Circuit connections (utilising line clamp)

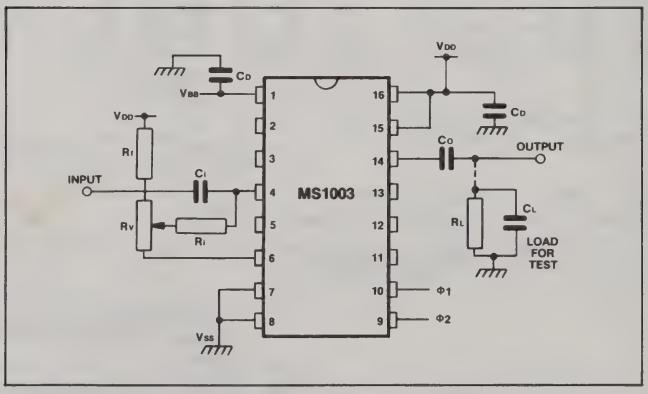


Fig.5 Circuit connections (line clamp disabled)

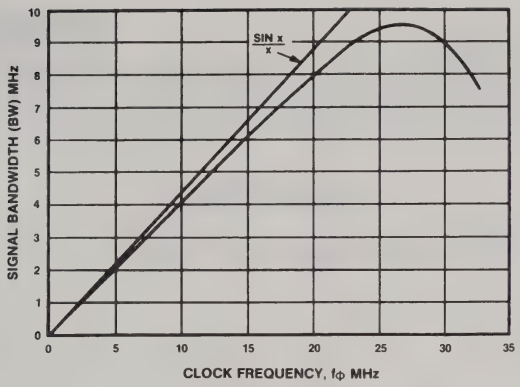


Fig.6 Typical bandwidth

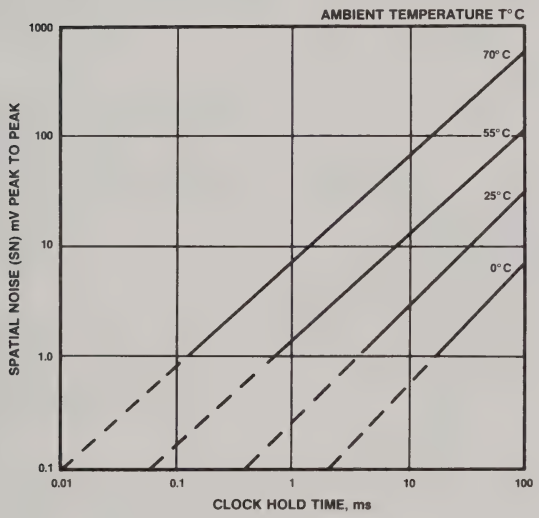


Fig.7 Typical output spatial noise as a function of clock hold time and operating temperature

PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MS1005

1024 ELEMENT CCD ANALOGUE STORE

The Plessey MS1005 is a clock controlled analogue shift register for applications including time delay, compression/expansion and temporary storage of analogue or digital signals. Information is transferred through the device by two externally supplied clocks; the timing between the clocks is not critical. A soft line clamp facility is available so that the input can be referenced to a desired voltage level. Internal thermal compensation circuits correct for any drift in CCD bias over a wide range of temperature.

FEATURES

- Typically 5MHz Video Bandwidth With A Clock Frequency of 13.3MHz
- 15V Supply Operation
- Internal Thermal Compensation To Correct For Any Drifts in CCD Input Bias
- Soft Line Clamp Facility

APPLICATIONS

- Electrically Variable Analogue Delay
- Time Base Correction
- Time Compression/Expansion
- Video Line Store

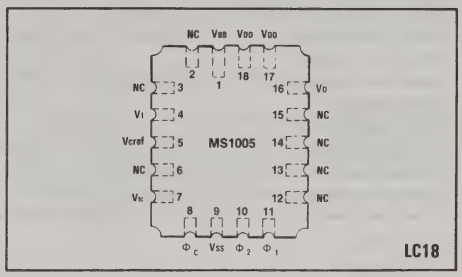


Fig.1 Pin connections - top view

PIN NAMES

V_{BB}	Substrate Bias
V_I	Analogue Input
V_{ref}	Clamp Reference Bias
V_{tc}	Thermal Compensation Bias
Φ_C	Clamp Pulse
V_{DD}	Drain Supply
V_O	Analogue Output
NC	Not Connected
Φ_1	Clock 1
Φ_2	Clock 2
V_{SS}	Ground

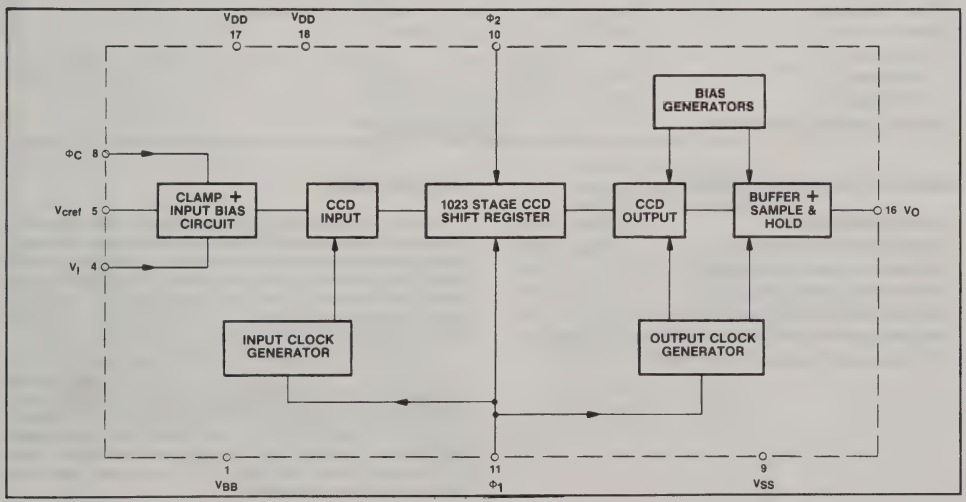


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{BIAS} = 4V, $\Phi_C = \Phi_{CL}$, V_{DD} = 15V, V_{BB} = -5V, Φ_L = 0.8V, Φ_H = 11.2V, fΦ = 13.3MHz, f_{sig} = 1kHz, T = 25°C

Characteristic	Symbol	Value			Units	Notes
		Min.	Typ.	Max.		
Supply current	I_{DD}		12	16	mA	$\Phi_1 = \Phi_H, \Phi_2 = \Phi_L$
Substrate current	I_{BB}		10	20	μA	
Gain	G	-2	0	+2	dB	V_{in} = 100mV pk/pk
Differential gain	ΔG			3	%	V_{in} = 1V pk/pk
Bandwidth	BW	4.5	5		MHz	V_{in} = 1V pk/pk
Random noise	RN			0.8	mV	Bandwidth = 4.5MHz
Spatial noise	SN			2.5	mV	Hold time = 1ms $\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Rate of output signal offset	RSO			3	mV/ms	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Output droop rate	V_O/T		4	8	V/s	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Signal input leakage	I_{in}		0.1		nA	
Signal input capacitance	C_{in}	4		7	pF	
Output resistance	R_O		0.4	1	kΩ	
Clock capacitance						
Phase/phase Φ_1/Φ_2	CΦ[1]		90	120	pF	
Phase/gnd	CΦ		75	100	pF	Φ_1 and Φ_2
Clamp capacitance	$C_{\Phi C}$	4		7	pF	
T = +70°C						
Spatial noise	SN			50	mV	Hold time = 1ms $\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Rate of output signal offset	RSO			70	mV/ms	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Output droop rate	V_O/T			200	V/s	$\Phi_1 = \Phi_L, \Phi_2 = \Phi_H$
Signal input leakage	I_{in}			100	nA	

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Value		Units	Notes
		Min.	Max.		
Supply voltage - positive	V_{DD}	14.5	15.5	V	
Substrate bias supply	V_{BB}	-6	-4	V	
Clock low	Φ_L	-1	0.8	V	All clock inputs
Clock high	Φ_H	11.2	V_{DD}	V	All clock inputs
Clamp low	Φ_{OL}	-1	0.8	V	
Clamp high	Φ_{CH}	11.0	V_{DD}	V	
Input bias range	V_{BIAS}	3.5	4.5	V	V_{in} = 100mV pk/pk
Clock frequency	fΦ	-	25	MHz	
Output load					
Resistance	R_L	10	-	kΩ	
Capacitance	C_L	-	15	pF	
Ambient operating temperature	T	0	70	°C	

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-65°C to +100°C
Ambient operating temperature	0°C to +70°C
Max.positive supply voltage (V_{DD})	+19V
Min.negative supply voltage (V_{BB})	-6V
Max.voltage on any pin (except V_{DD}, V_{BB})	V_{DD}
Min.voltage on any pin (except V_{DD}, V_{BB})	V_{BB} -0.3V
All voltages with respect to V_{SS} (Ground)	

PRECAUTIONS

This device has limited immunity to static electricity when handled. The conductive foam or plastic carrier provided should be retained until the device is incorporated in its circuit. Any handling of the device without its plastic carrier should be minimised. Care should be taken to avoid any static discharges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

Care should also be taken to avoid voltage transients in the supply leads. These can occur when the supplies are switched on or off. The track length from the clock drivers to the CCD store should be minimised to prevent overshoots on the clock waveforms. It is permissible to allow these overshoots to exceed the minimum and maximum clock voltage specifications by up to 2V for not longer than 10ns duration per clock transition.

GENERAL OPERATION

The circuit operates as a sampled shift register under the control of the external clocks Φ_1 and Φ_2. Analogue input signals are sampled on the falling edge of the Φ_1 clock and are subsequently stored and shifted through the device to appear at the output after 1024 complete clock cycles (see timing diagram in Fig.3 for exact delay information). Each output sample is presented on the falling edge of Φ_1 and exists for an entire clock period. The output waveform consists of the delayed and/or stored analogue information plus components of the inverse Φ_1 clock due to breakthrough from internal sample and hold circuits. Connections for two-phase operation are shown in Fig.4. If the soft line clamp facility is not desired, it may be disabled by connecting Φ_C to V_{SS}. In this case, to maintain correct input biassing, the wiper of R_V should be connected to pin 4 instead, via a resistor, as shown in Fig.5. The device exhibits signal inversion.

Delay mode

Incoming signals are applied to the terminal V_I via a coupling capacitor (Fig.4). It is necessary for the user to ensure that the incoming analogue signal contains no frequency components in excess of $f\Phi \div 2$ in order to avoid spurious components, due to aliassing, appearing at the output. The output waveform is available directly from the device, or may be taken via a suitable buffer circuit if a lower output impedance is required. Analogue information appears at the output terminal delayed in time by 1024 clock cycles. The frequency response characteristics of the device are related to the clock frequency, $f\Phi$ as shown in Fig.6.

The clock frequency is variable over a wide range. At high frequencies ($>$ 25MHz) the bandwidth of the device becomes limited owing to the decreasing efficiency of the charge coupled shift register. At low frequencies ($<$ 100kHz) the signal range is diminished because of the generation of thermal charge in the shift register; hence the minimum clock frequency is related to the maximum operating temperature (the 100kHz figure corresponding to 70° C operation). The device should be located away from circuit components which dissipate power and should be provided with the coolest ambient offered by the system. Heat dissipation from the analogue store itself may be assisted by soldering uncommitted pins to an earth plane. At low frequencies the effects of thermally generated currents can be minimised by using clocks having a short Φ_1 on-duration ($t_2 \approx$ 100ns). This approach also simplifies the filtering of clock noise from the output. A 100nF decoupling capacitor on pin 6 may be necessary in some applications.

Time compression/expansion

Compression or expansion of analogue signals in the time domain may be achieved by loading and unloading the shift register at different frequencies. The low frequency limit for this mode of operation is dictated by the rate of average signal offset (RSO) as this will reduce the maximum output signal amplitude.

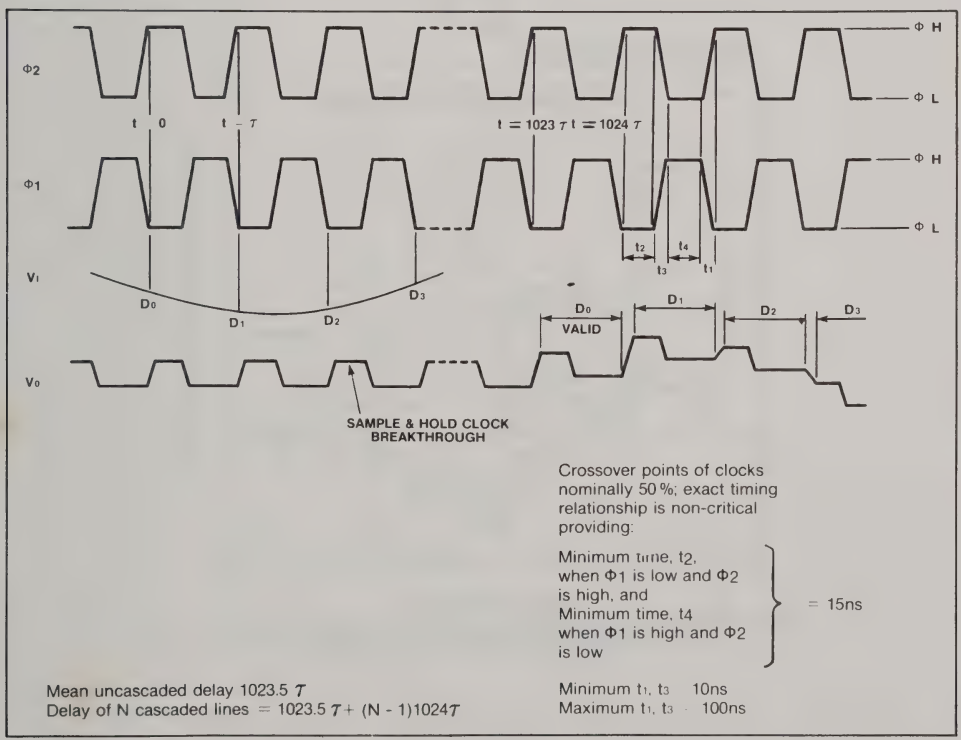


Fig.3 Timing diagram

Analogue storage

When the shift register has been loaded with analogue signals, the clocks may be interrupted to achieve temporary storage of the information. The samples are retrieved when the clocks are subsequently re-started. The clocks must be stopped in the state $\Phi_1 = \Phi_L$ in order to minimise degradation of the signal due to thermal leakage currents. The maximum hold time is determined by the spatial noise parameter (SN). Spatial noise magnitude is a function of stop clock period and of operating temperature as shown in Fig.7.

Component values

C_O	Output Capacitor, 1.0μF	
C_i	Input Capacitor, 0.1μF	
R_i	Input Resistor, 47kΩ	
R_V	Variable Resistor, 200kΩ	
R_f	Fixed Resistor, 820kΩ	
R_L	Load Resistor, 10kΩ	(including measuring
C_L	Load Capacitor, 15pF	kit impedance)
C_D	Decoupling Capacitors, 10nF	

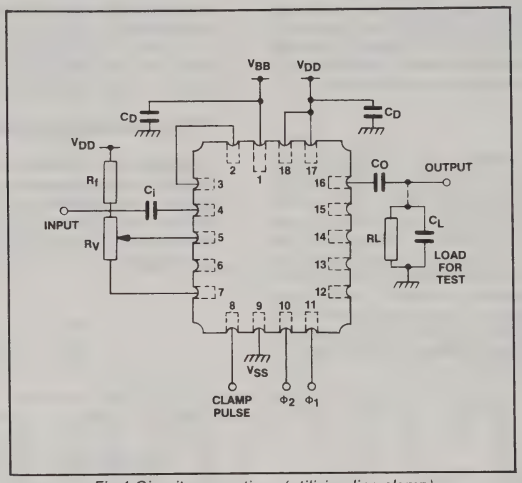


Fig.4 Circuit connections (utilising line clamp)

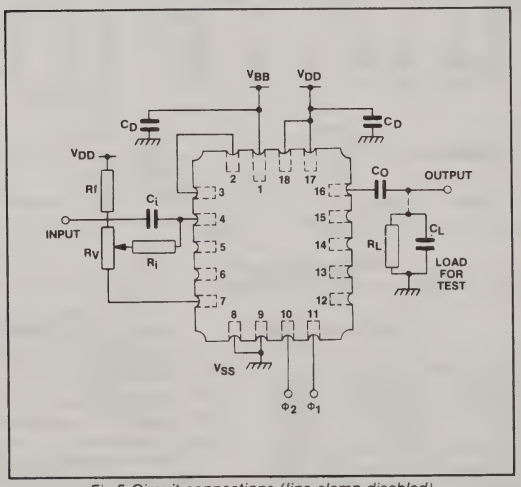


Fig.5 Circuit connections (line clamp disabled)

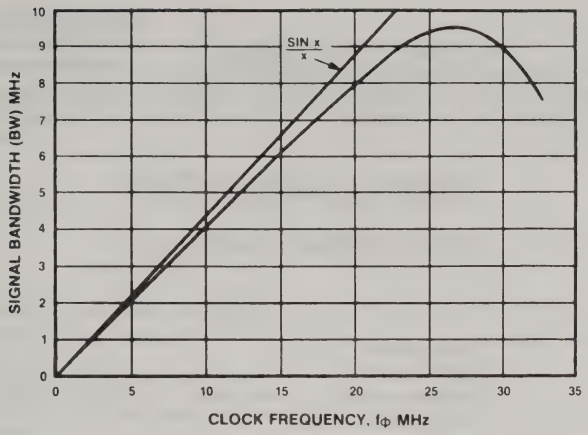


Fig.6 Typical bandwidth

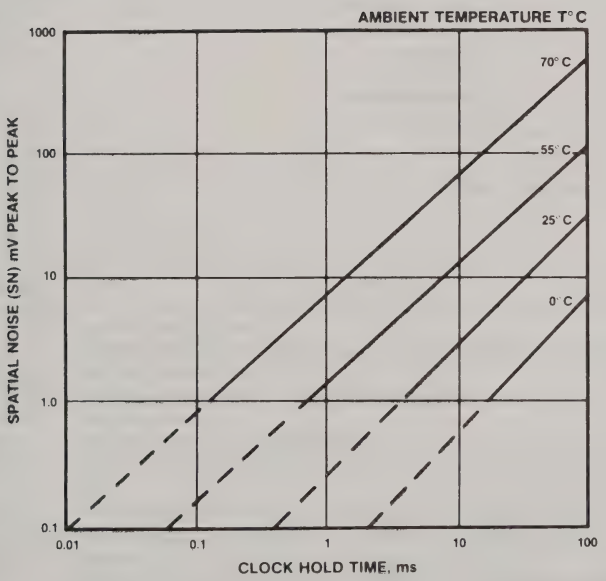


Fig.7 Typical output spatial noise as a function of clock hold time and operating temperature

PLESSEY Semiconductors — ADVANCE INFORMATION — TELEVIEW

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

PIC1650-532/533

TELEVIEW CONTROL CHIP

The Teleview control chip, PIC1650-532/533 interfaces the user to the Teleview system and generally organises the operation of the system.

It is available in several versions each providing alternative user inputs and operating features. Customised versions can be provided if required. The details of the various versions are shown in this datasheet.

FEATURES

- Interfaces User to Teleview System
- Initialises Teleview System
- PIC1650-532 ASCII or Binary (IR Remote), Initialises to Picture Mode
- PIC1650A-533 ASCII or IR Remote, Viewdata only, Local Programming of EAROM

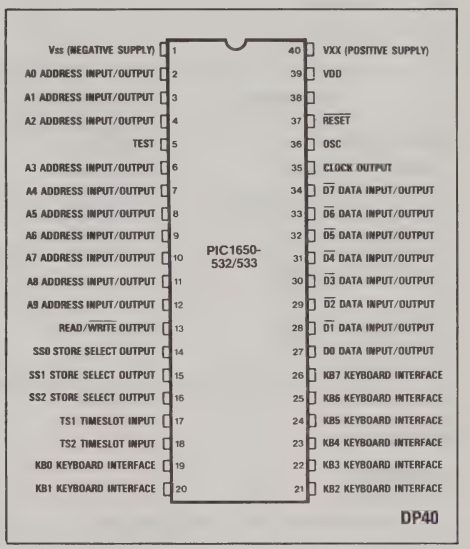


Fig.1 Pin connections - top view

PIN FUNCTIONS

Pin Number	Name	Function
1	Vss	Negative supply (Ground)
2-12	A0-A9	Address Input/Outputs which are connected to the Teleview Address Bus
5	Test	Test pin - connect to Vss
13	Read/Write	Control output connected to the Teleview Store R/$\overline{W}$ input
14-16	SS0-SS2	Store Select outputs
17,18	TS1,TS2	Time Slot Inputs from Video Generator
19-26	KB0-KB7	Keyboard Interface, may be Inputs, Outputs or Inputs/Outputs depending on the version
27-34	$\overline{D0}$-$\overline{D7}$	Data Inputs/Outputs which are connected to the Teleview Data Bus
35	Clock Output	Not used except to check the Clock frequency (output frequency fc/4)
36	Oscillator	Oscillator resistor and capacitor connected to this pin
37	$\overline{\text{Reset}}$	Master reset input which must be kept at ground potential until the VDD power is within specification
38		Not used
39	VDD	Positive power supplies +5V Nom.
40	VXX	

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to Vss pin . . . . . –0.3V to +15V
Ambient operating temperature range . . . . . 0°C to +70°C
Storage temperature range . . . . . –55°C to +150°C

Exceeding these ratings could cause permanent damage. Functional operation is not guaranteed under these conditions. Operating ranges are specified below.

ELECTRICAL CHARACTERISTICS (See PIC1650A Date Sheet for full specification).

Standard conditions (unless otherwise stated)

VSS = 0V
VDD = +5V ±10%
VXX = +5V ±10%
F clock = 1MHz
Ta = 0°C to +70°C

Characteristic	Min.	Typ	Max	Units	Conditions
Clock Frequency	0.8		1.0	MHz	
Input Low Voltage	–0.2		0.8	V	
Input High Voltage	2.4			V	
Input High Voltage $\overline{(Reset)}$	Vdd–1			V	
Input Low Current	–200		–1600	μA	VIL = 0.4V
Input High Current	–100			μA	VIH = 2.4V
Input Leakage Current $\overline{(Reset)}$	–10		10	μA	
Output Low Voltage			0.4	V	IOL = 1.6 mA
Output High Voltage	2.4			V	IOH = –100μA
Supply Current			60	mA	IDD + IXX

PIC1650-532

APPENDIX 1

This version interfaces either with an ASCII return to zero keyboard or from remote control receiver data.

INPUT
(a) ASCII Return to zero
(b) Binary Return to zero (from local keyboard or remote control)

POWER UP MODE
Picture

POWER UP DISPLAY
(a) ASCII — Teleview Cyan
(b) Binary — Teleview Yellow

POWER UP PAGE
XOO in Store 7

KEYBOARD INTERFACE

KB0 pin 19	LSB Input
KB1 pin 20	LSB Input
KB2 pin 21	LSB Input
KB3 pin 22	LSB Input
KB4 pin 23	LSB Input
KB5 pin 24	LSB Input
KB6 pin 25	MSB Input
KB7 pin 26	ASCII/Local Binary Input or Remote Acknowledge

KEYBOARD CODES

(a) ASC II Standard 7 bit ASCII (These codes are only acted upon in Viewdata Mode)
(b) Binary (Local or Remote)

Binary Code MSB LSB	Key Meaning
1 1 0 0 0 0 0	Picture/Text
1 1 0 0 0 0 1	Mix
1 1 0 0 0 1 0	Half Page Expansion
1 1 0 0 0 1 1	Store Select
1 1 0 0 1 0 0	7
1 1 0 0 1 0 1	8
1 1 0 0 1 1 0	9
1 1 0 0 1 1 1	Box Clock
1 1 0 1 0 0 0	4
1 1 0 1 0 0 1	5
1 1 0 1 0 1 0	6
1 1 0 1 0 1 1	Hold (Store Rotating Pages) (Release Line)
1 1 0 1 1 0 0	1
1 1 0 1 1 0 1	2
1 1 0 1 1 1 0	3
1 1 0 1 1 1 1	Reveal/Conceal
1 1 1 0 0 0 0	Page (or * in Viewdata)
1 1 1 0 0 0 1	0
1 1 1 0 0 1 0	Time (or # in Viewdata)
1 1 1 0 0 1 1	Update/Clear
1 1 1 0 1 0 0	Rounding + Flash Off
1 1 1 0 1 0 1	Cursor ON
1 1 1 0 1 1 0	Cursor OFF
1 1 1 0 1 1 1	Roll Headers

PIC1650A-533

APPENDIX 2

This version interfaces either with an ASCII, return to zero keyboard or with a remote control receiver and as such may replace pattern 532.

It provides control of Viewdata functions only together with Local Programming of Telephone numbers via PIC1650Z-536.

INPUT ASCII return to zero or binary return to zero from local keyboard or direct connection to remote receiver.

POWER UP MODE Text, Cursor off

POWER UP DISPLAY Double height Teleview in yellow on blue

POWER UP STORE Store number 1 (binary 000)

KEYBOARD INTERFACE

KB0 pin 19	LSB Input
KB1 pin 20	LSB Input
KB2 pin 21	LSB Input
KB3 pin 22	LSB Input
KB4 pin 23	LSB Input
KB5 pin 24	LSB Input
KB6 pin 25	MSB Input
KB7 pin 26	ASCII/Local Binary Input or Remote Acknowledge

KEYBOARD CODES

(a) ASCII — Full 7 bit ASCII set

(b) Binary (local or remote)

Binary Code	Key Meaning
1100000	Picture/Text
1100001	Print
1100010	Half Page Expansion
1100011	Store Select
1100100	7
1100101	8
1100110	9
1100111	(Not Used)
1101000	4
1101001	5
1101010	6
1101011	Hold/Disconnect Line
1101100	1
1101101	2
1101110	3
1101111	Reveal/Conceal
1110000	Star
1110001	0
1110010	Square
1110011	Clear (Inhibit Display)
1110100	Rounding & Flashing Off
1110101	Cursor On
1110110	Cursor Off
1110111	Reset

Notes 1 and 2 as for pattern 532.

OPERATION

(a) ASCII codes transmitted directly to line via UAR/T and MODEM. If 536 autodialler fitted, square and digits 1-4 will enable dialling.

(b) Picture/Text. Switches display alternately between picture and text. If 536 autodialler fitted this key will drop the telephone connection.

(c) Print. Alternately puts system into MIX mode and back to normal. Mix mode enables monochrome video to be generated and removes coloured backgrounds. When entering mix mode character rounding and flashing are inhibited until new page received (only for MR9735).

(d) Store/Select. Followed by digits 1-8 will select one of eight possible Stores for display. If 536 autodialler fitted and system in 'link-back' mode then Local Programming of telephone numbers may be enabled by selecting zero. SS0 will clear screen and digits 1-4 may be pressed to enable the programming of the appropriate telephone number. The number is entered using digits 0-9 (0 displayed as :) star for access pause (displayed as ;) and square as formatter and space filler (displayed as ?) to complete all 16 digits. SS0 followed by Reveal will display all the telephone numbers on the screen.

(e) Hold. If the 536 autodialler is fitted this key will drop the telephone line.

(f) Reveal/Conceal. Will alternately reveal and conceal characters. Initialised to conceal state for new page or new Store.

(g) Clear. Clears the screen of all text. Display restored by second depression of the key and by reception of a new page.

(h) Rounding and Flashing Off. Character rounding and flashing may be inhibited in MR9735 until a new page is received.

(i) Cursor ON/OFF. The cursor may be locally controlled by these codes.

(j) Reset. Simulate the power-on reset. All stores are cleared and initialised to 'Teleview'.

Notes:

During initialisation the PIC1650-532/533 decides whether an ASCII keyboard or a remote control receiver is being used. If all Keyboard Interface inputs are low an ASCII keyboard is assumed.

1.(a) **ASCII Mode**

Return to zero signalling is employed, the KB7 input being used to switch from full ASCII to local Binary.

With KB7 equal to 1 the other 7 bits are read as standard ASCII. (Note this input must be pulsed with the other bits).

With KB7 equal to 0 the other 7 bits are read as binary with meanings detailed above.

(b) **Remote Mode**

In this case the same binary codes are used but an acknowledgement routine is performed by the PIC1650-532/533.

The connections between the PIC1650-532/533 and a remote control receiver are made as follows:

PIC1650-532	REMOTE CONTROL WORD
KB0 pin 19	LSB CODE BIT A
KB1 pin 20	CODE BIT B
KB2 pin 21	CODE BIT C
KB3 pin 22	CODE BIT D
KB4 pin 23	CODE BIT E
KB5 pin 24	CODE BIT F
KB6 pin 25	MSB CODE BIT G
KB7 pin 26	ACKNOWLEDGE SIGNAL

2. The codes should be valid for a minimum of 20msecs. In the ASCII mode if two key operation SS0 is used the Second code (0) should only be valid for a maximum of 120ms to avoid changing keyboard modes (see Application Notes).

3. The double key operations are recognised:

   (a) Store Select 9 is equivalent to Roll Headers.

   (b) Store Select 0 is equivalent to Reset (Clear Stores).

APPLICATION NOTES

Figs. 2, 3 and 4 show circuit diagrams of three options for signalling via the keyboard interface. Those of Figs. 2 and 3 use the ASCII return-to-zero mode for remote or local applications.

One point to note is that the extra logic based around a NAND latch provides an enable/disable feature for the remote option: a transmitted 11111 code from the SL490 allows subsequent codes to communicate with the PIC1650-532. A transmitted 11011 code disables communication and thus allows bits 1 to 6 (KB0 to KB5) to be used again for signalling to other devices i.e. the PIC1650-532 will ignore all subsequent codes since KB6 (pin 25) is held low as a result of the 'disable' code.

The enable/disable codes can be changed by alternating the connections to the 4 I/P AND gate driving the NAND latch, or omitted altogether by connecting KB6 to KB5 in common with the drive to KB5.

To signal in remote mode (and thereby avoid the condition referred to in Note 2 above) simple extra logic as shown in Fig.4 can be employed. The KB7 pin is pulsed low by the PIC1650-532 operation every 20ms, and this is used to drive a simple NAND latch which forms an acknowledgement-type function with the ML924 outputs. Note that omitting the enable/disable feature is still possible as before, simplifying the AND gate driving KB5 and KB6 to a 2-input gate.

Similar logic can of course be employed for a local keypad using Remote mode.

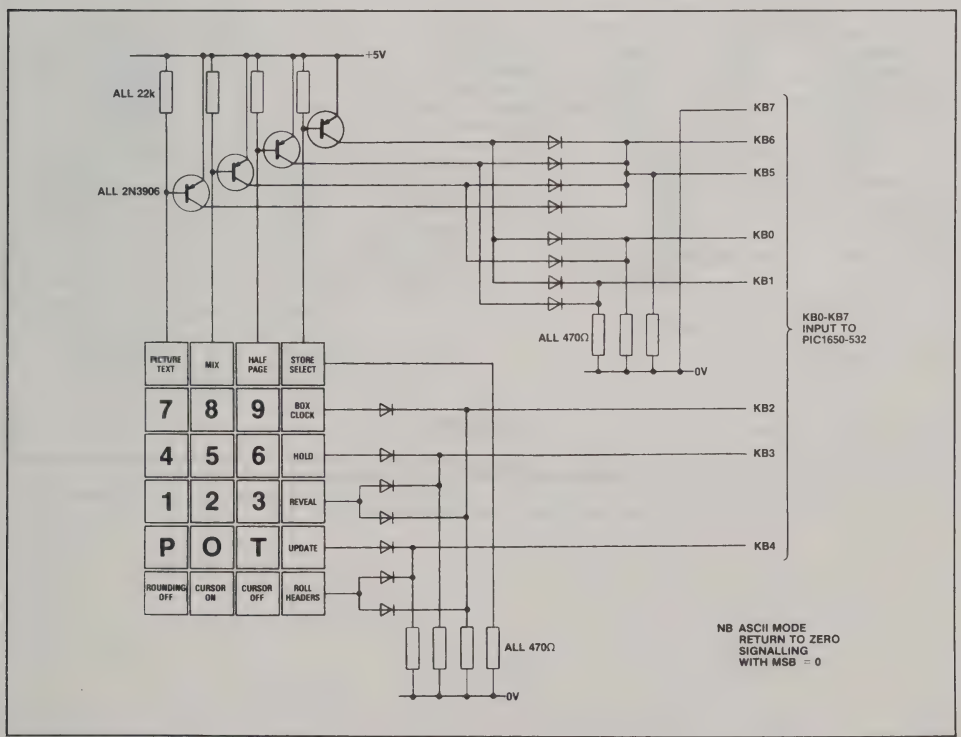


Fig.2 Local keypad using ASCII mode signalling

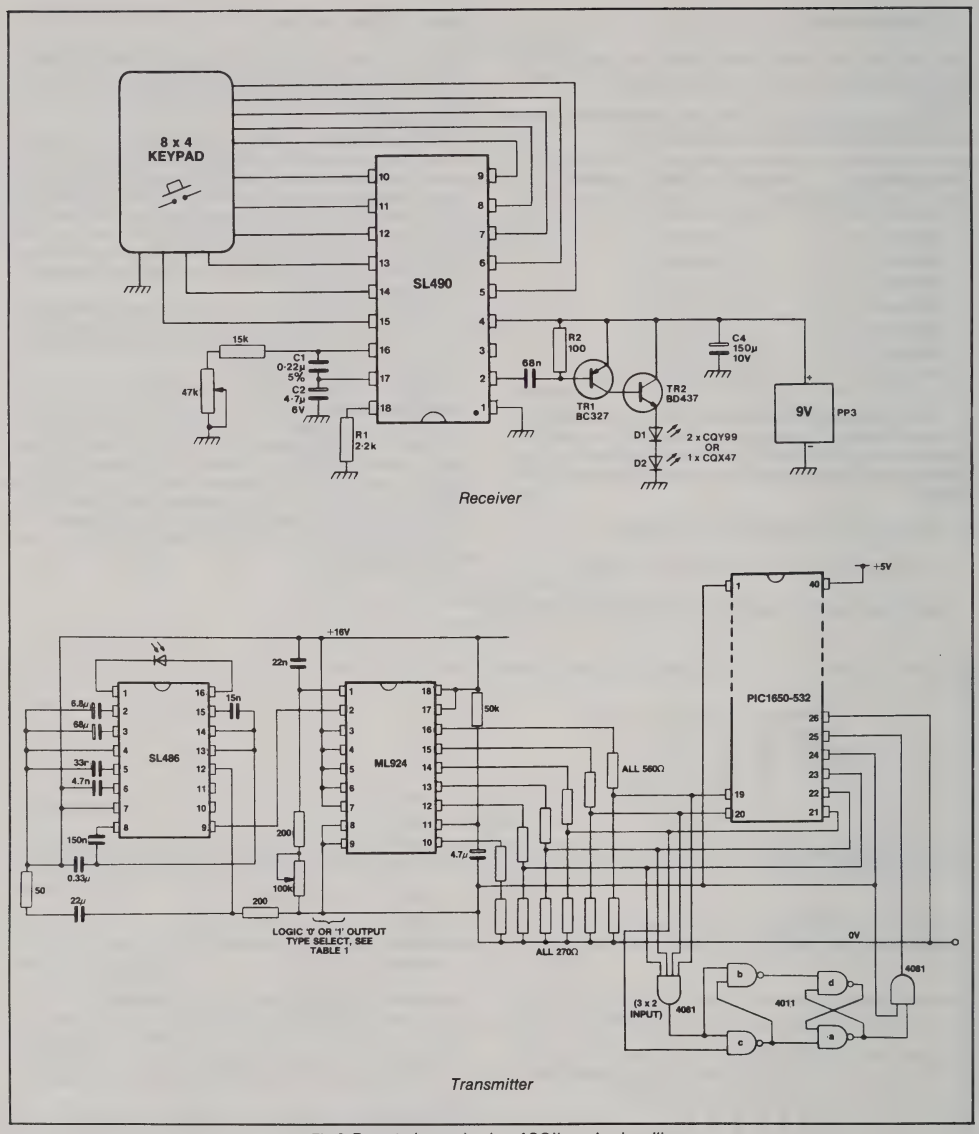


Fig.3 Remote keypad using ASCII mode signalling

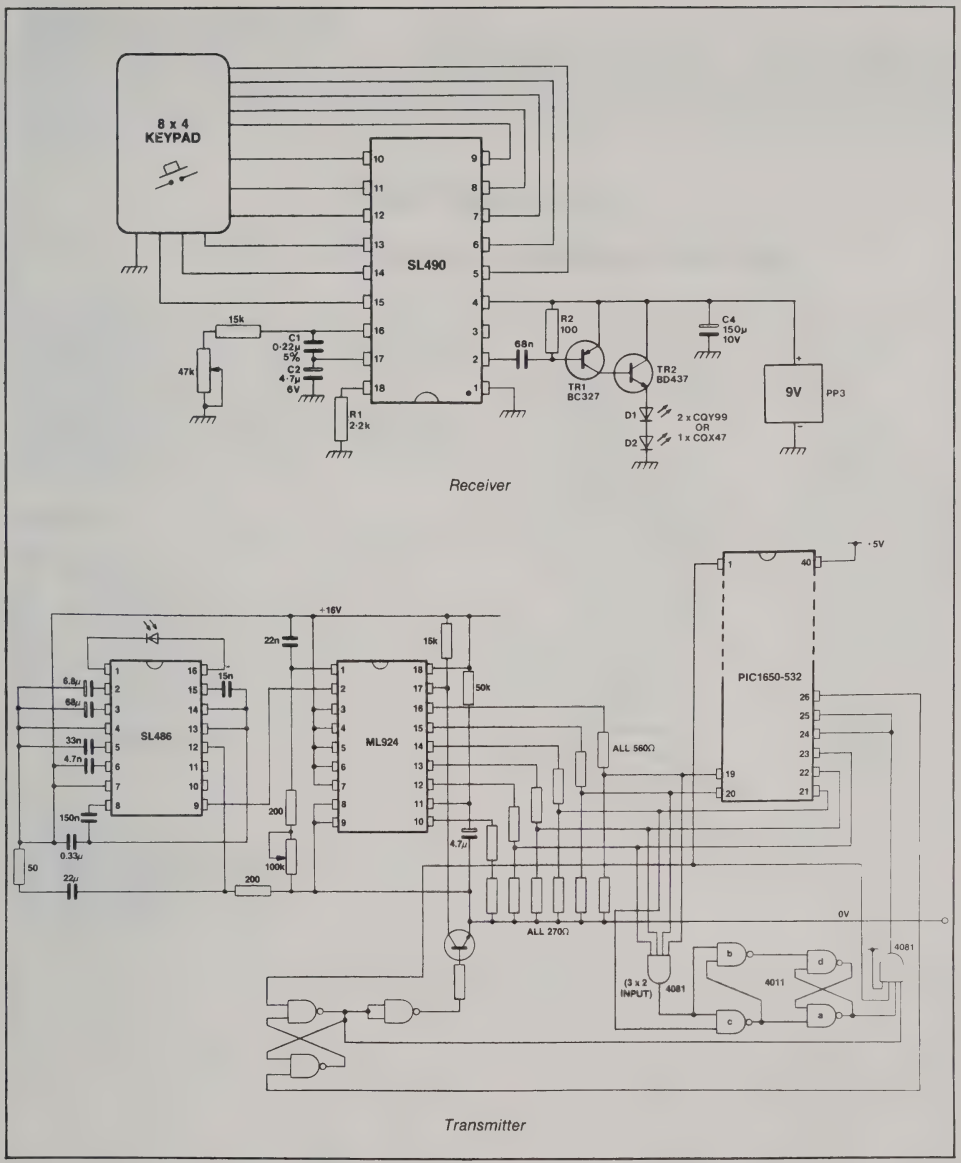


Fig.4 Remote keypad using remote mode signalling

PLESSEY Semiconductors — ADVANCE INFORMATION — TELEVIEW

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

PIC1650-536

TELEVIEW AUTODIALLER/TERMINAL IDENTIFIER

The Autodialler/Terminal Identifier is an extension to the TELEVIEW system that is designed to perform the Autodialling function of a Viewdata system, to transmit the terminal identification (ID) code and to allow the remote programming of all the stored numbers.

The system consists of a PIC1650-536 attached to the TELEVIEW address and data highways, an EAROM for non-volatile storage of the ID and telephone numbers and relays for controlling the telephone line.

FEATURES

- Non-volatile Storage of 4 Telephone Numbers of 16 Digits
- 10 IPS Loop Disconnect Dialling
- Non-Volatile Storage of Identity Code of 16 Digits
- Full Remote Programming Capability
- Optional Local Programming
- Easy Connection to Teleview System
- Spare memory locations

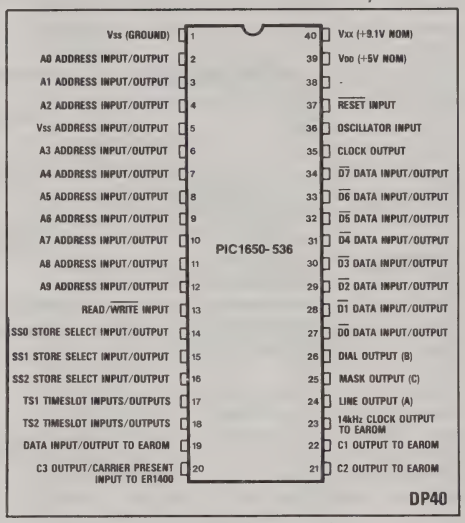

Vss (GROUND) 1
A0 ADDRESS INPUT/OUTPUT 2
A1 ADDRESS INPUT/OUTPUT 3
A2 ADDRESS INPUT/OUTPUT 4
Vss ADDRESS INPUT/OUTPUT 5
A3 ADDRESS INPUT/OUTPUT 6
A4 ADDRESS INPUT/OUTPUT 7
A5 ADDRESS INPUT/OUTPUT 8
A6 ADDRESS INPUT/OUTPUT 9
A7 ADDRESS INPUT/OUTPUT 10
A8 ADDRESS INPUT/OUTPUT 11
A9 ADDRESS INPUT/OUTPUT 12
READ/WRITE INPUT 13
SS0 STORE SELECT INPUT/OUTPUT 14
SS1 STORE SELECT INPUT/OUTPUT 15
SS2 STORE SELECT INPUT/OUTPUT 16
TS1 TIMESLOT INPUTS/OUTPUTS 17
TS2 TIMESLOT INPUTS/OUTPUTS 18
DATA INPUT/OUTPUT TO EAROM 19
C3 OUTPUT/CARRIER PRESENT INPUT TO ER1400 20
PIC1650-536
40 Vxx (+9.1V NOM)
39 Voo (+5V NOM)
38 -
37 RESET INPUT
36 OSCILLATOR INPUT
35 CLOCK OUTPUT
34 D7 DATA INPUT/OUTPUT
33 D6 DATA INPUT/OUTPUT
32 D5 DATA INPUT/OUTPUT
31 D4 DATA INPUT/OUTPUT
30 D3 DATA INPUT/OUTPUT
29 D2 DATA INPUT/OUTPUT
28 D1 DATA INPUT/OUTPUT
27 D0 DATA INPUT/OUTPUT
26 DIAL OUTPUT (B)
25 MASK OUTPUT (C)
24 LINE OUTPUT (A)
23 14kHz CLOCK OUTPUT TO EAROM
22 C1 OUTPUT TO EAROM
21 C2 OUTPUT TO EAROM
DP40

Fig.1 Pin connections - top view

PACKAGE

PIC1650-536 — 40 lead DIL

ABSOLUTE MAXIMUM RATINGS

See PIC1650 datasheet for details.

ELECTRICAL CHARACTERISTICS

See PIC1650 datasheet for details.

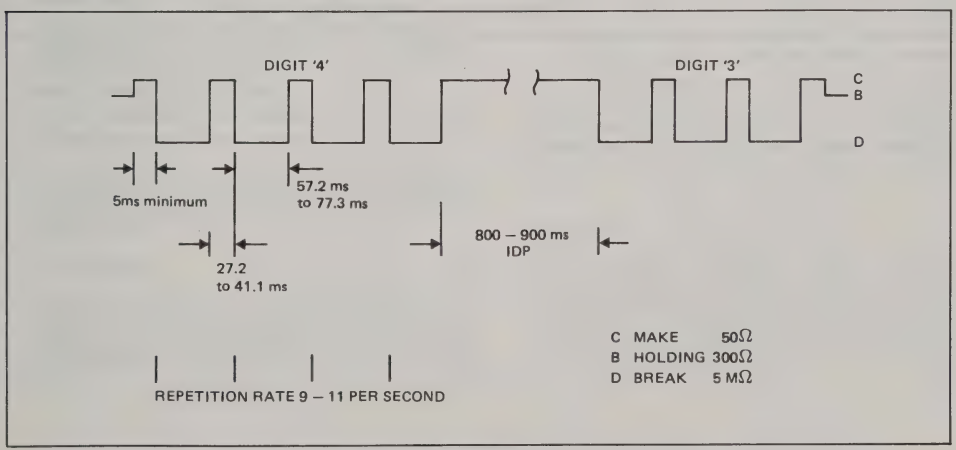


Fig.2 Autodialler pulses

PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
PIC1650-536		
1	V_{SS}	Ground
2	A0	Address Input/Output - connect to TELEVIEW Address Bus
3	A1	
4	A2	
5	V_{SS}	
6	A3	Address Input/Output - connect to TELEVIEW Address Bus
7	A4	
8	A5	
9	A6	
10	A7	
11	A8	
12	A9	
13	Read/$\overline{\text{Write}}$ Input/Output	Control to Page Memory - connect to TELEVIEW R/W line
14	SS0	Store Select Inputs/Outputs - connect to TELEVIEW SS lines
15	SS1	
16	SS2	
17	TS1	Time Slot Inputs - connect to TELEVIEW TS lines
18	TS2	
19	Data Input/Output	Interface to EAROM non volatile memory. Pin 20 doubles as the carrier present input.
20	C3 Output	
21	C2 Output	
22	C1 Output	
23	14kHz Clock Output	
24	Line Output (A)	Output to Line Looping relay
25	Mask Output (C)	Output to Mask relay
26	Dial Output (B)	Output to Dialling relay
27	$\overline{D0}$	Data Input/Output - connect to TELEVIEW Data Bus
28	$\overline{D1}$	
29	$\overline{D2}$	
30	$\overline{D3}$	
31	$\overline{D4}$	
32	$\overline{D5}$	
33	$\overline{D6}$	
34	$\overline{D7}$	
35	Clock Output	Monitor point for Clock oscillator. Set frequency to 250kHz nominal
36	Oscillator Input	Connect Clock oscillator components to this point
37	$\overline{\text{Reset}}$ Input	Master reset input connect to corresponding pin on TELEVIEW control PIC1650.
38	-	No connection
39	V_{DD}	Positive supply +5V nom.
40	V_{XX}	Positive supply to output buffers +9.1V nom.

OPERATION

Autodialler

The system responds to inputs via the TELEVIEW keyboard in order to initiate the automatic dialling of the Viewdata telephone numbers. There are 4 stored telephone numbers that may be accessed by 4 keys as described in the Prestel Terminal Specification.

Each Telephone number can consist of up to 16 digits including access pauses and formatting codes.

The system may be operated fully automatically or with manual dialling.

1. Automatic Dialling

With the system off-line and in the Viewdata mode the initial action is to press the Square (#) key. The Televiev system will be put in the Text mode and the currently displayed Store will be cleared. The telephone line will be looped and the audio should be switched to a loudspeaker.

Once dialling tone is heard a digit is pressed according to the Viewdata service required.

Digit 1 – will give the Prestel service. (Block 2)

Digit 2 – will give a second number for the Prestel service. (Block 3)

Digit 3 – will give the third number. (Block 6)

Digit 4 – will give the fourth number. (Block 7)

If a digit is not pressed for 30 seconds after the Square (#) key the line will be released. The digits will be put onto the screen as they are being dialled and if formatting characters had been loaded in the digit store the display will be spaced accordingly.

If a pause had been programmed, for access to a further dial tone for example, the system will put a * on the screen and wait for release. To release the access pause the appropriate digit is pressed again and dialling will continue. If the system does not receive a manual release it will continue after a time-out of four seconds.

If at the end of dialling the call fails, pressing the Square (#) key will clear the call and then start again by re-looping the line.

When the required incoming carrier tone is received the modem will return its appropriate tone to the Viewdata computer which may then send the first page of data and initiate terminal identification.

If the carrier tone is not received for any reason the line will be released after 30 seconds.

Once a satisfactory connection is made to the Viewdata computer (i.e. carrier is detected), the keypad will revert to normal Viewdata mode and dialling will not be possible.

2. Manual Dialling

If the required telephone number is not stored within the terminal the call may be made using the normal telephone. The system should start off-line and in the Viewdata mode. The number is dialled using the telephone in the normal way and when dialling is complete the Square (#) Key is pressed. This will put the system into the Text mode, erase the currently displayed store and hold the line. The telephone handset is replaced and once the carrier tone is received the procedure is as before.

3. Connection Release

If at any time the carrier detection logic detects that the carrier is lost the connection will be immediately released.

The connection will also be released when the Televiev system is switched to the Picture or Teletext modes, or if the Hold Key is pressed (if available).

Alternatively the appropriate computer log off procedure may be used.

In all cases the content of the Televiev Stores will remain as they were at the moment of disconnection.

5. Remote Programming

The Televiev highways will be monitored for those special ESC sequence codes that indicate the entry into the Programme-Verify mode as described in the Prestel Terminal Specification.

In the Televiev System the Data Acquistion chip receives data from the Viewdata computer and normally loads data to the display store. Any codes, particularly ESC sequences, that it does not use, it puts out onto the Televiev highway system where the remote programming device may receive them.

The basic programming sequences are as described in the Prestel Specification except that the data for programming the EAROM will initially be put into the display store by the DA chip. The programming device will read the digits from this store and erase them after checking that they are all valid codes. The display will be blanked during programming.

6. Local Programming

For system security, particularly in the domestic environment, the local programming of telephone numbers and identity codes is not encouraged.

However, the Televiev system has been designed such that it may "talk to itself" and by doing this and having some additional keys (especially ESC, ENQ, ?, : and ;) a very secure local programming mode is available.

The UAR/T transmit and receive clocks are connected to a single frequency, the output joined to the input and the carrier present input is forced true. The standard programming sequences may then be input to the system to read out and/or modify the content of the digit store.

7. Spare Storage

While only the first 7 blocks of storage are defined (as ID code plus 6 telephone numbers) a further 4 blocks are available and may be accessed by the Programme/Verify sequences if required. They could, for example, be used to store alternative identity/security codes for private Viewdata systems.

8. Programming Routine

(The following is an extract from the Prestel Terminal Specification).

The programming Routine is entered by a 4 character sequence ESC1 ESC2. This puts the terminal into Programme-Verify mode (See Fig. 3). The memory is divided into seven 16 character blocks. A skip block command ESC 3 is used to skip through the blocks. Default is block 1 at entry to Programme-Verify mode. After a number (0–6) of skip block commands, Verify mode may be selected by ENQ, or Programme mode may be selected by ESC 4.

Entry of Verify mode shall cause the terminal to transmit down the telephone line the contents of the current block (excluding any space-filling characters) and 75 bit/s and then revert to normal mode.

Programme data shall follow ESC 4 using the numbers 0–9 for the Identity Code and the codes given below for telephone numbers. Character 3/15 (?) will be used as a space filling character after valid data characters to make the total number of characters in a block equal to 16. 3/15 (?) may also be used between parts of the number to identify "natural" breaks. It may then be displayed as a space if the number is displayed for the user, e.g. :1?618?1111????? displayed as 01 618 1111. After recieving these 16 characters the terminal reverts to normal mode.

Dialler Codes DIALLED DIGIT	(only for blocks 2–7) RECEIVED IS07 CHARACTER (also used for transmission after ENQ for block verification)
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
0	:
PAUSE	;
RESERVED	<
SPACE FILLER	?

A delay of at least 5s will be present between the last character to be written into the memory and the next attempt to leave Normal mode. This is to facilitate the use of slow write/erase memories.

Blocks 1–7 are defined as follows:–

Block 1	Identity Number
Block 2	Telephone Number A
Block 3	Telephone Number B
Block 4	Not used
Block 5	Not used
Block 6	Telephone Number E
Block 7	Telephone Number F

A and B are the Prestel Computer Centre telephone numbers.

E and F are the third and fourth choices.

9. Line Interface

(The following is an extract from the Prestel Terminal Specification).

Physical Termination

British Telecom will install a Jack 96A in customers premises to access Prestel. The customer Prestel Terminal will require a suitable compatible plug (e.g. British Telecom Plug 505).

DC CONDITIONS

Four sets of DC conditions are specified for the line interface.

(a) The off-line condition (idle state) applies when the terminal is not using the telephone line.

(b) The line holding condition applies when the terminal goes on-line, is sending tones to or receiving tones from the line and during inter-digit pauses.

(c) The pulsing make condition applies during the make part of a dialled digit pulse.

(d) The pulsing break condition applies during the break-part of a dialled digit pulse.

		Plug Points	Resistance	Capacitance
(a)	Off-Line	2–3	> 5 Mohm*	⩽ 0.01μF
	Idle Condition	1–5	< 10 ohm	
(b)	Line Holding	2–3	⩽300 ohm+	
	Condition	1–5	> 5 Mohm	
(c)	Pulsing Make	2–3	⩽ 50 ohm	
		1–5	> 5 Mohm	
(d)	Pulsing Break	2–3	> 5 Mohm	
		1–5	> 5 Mohm*	
	All times	Any to earth	> 5 Mohm*	⩽ 0.01μF

* Measured at 250V DC. All conditions to be independent of polarity.

\+ Measured with line currents up to 120 mA.

The max DC short circuit available from line is 120mA.

AC CONDITIONS

When the terminal is on-line (i.e. line holding condition) it shall present an impedance between 400 and 900 ohms at an angle not greater than 45 degrees for all frequencies between 300Hz and 3400Hz between plug points 2 and 3.

AUTODIALLING

If a loop disconnect autodialler is fitted then the following requirements must be met:

The digit signals shall appear as loop disconnect pulses between Plug Points 2 and 3 at a repetition rate of between 9 and 11 pulses per second. The break period shall be

between 63% and 70% of the total pulse period (break plus make). The length of the break period condition (d) of each pulse shall be within the limits of 57.2 to 77.3 ms and the length of the make period condition (c) between any two break periods shall be within the limits 27.2 to 41.1 ms. For a period of at least 5 ms before and after pulsing condition (c) shall apply.

The digit to be dialled represents the number of break pulses to be sent except that digit 0 represents 10 pulses.

Inter digit pauses shall be provided. The duration shall be between 800 and 900 ms. During the pause, condition (b) shall apply except during the first and last 5 ms periods when condition (c) shall apply. Fig. 2 explains this diagramatically.

When the terminal is transferring to the line holding state the high impedance between Plug Points 1 and 5 must not be presented more than 20 ms before the low impedance is presented between Plug Points 2 and 3.

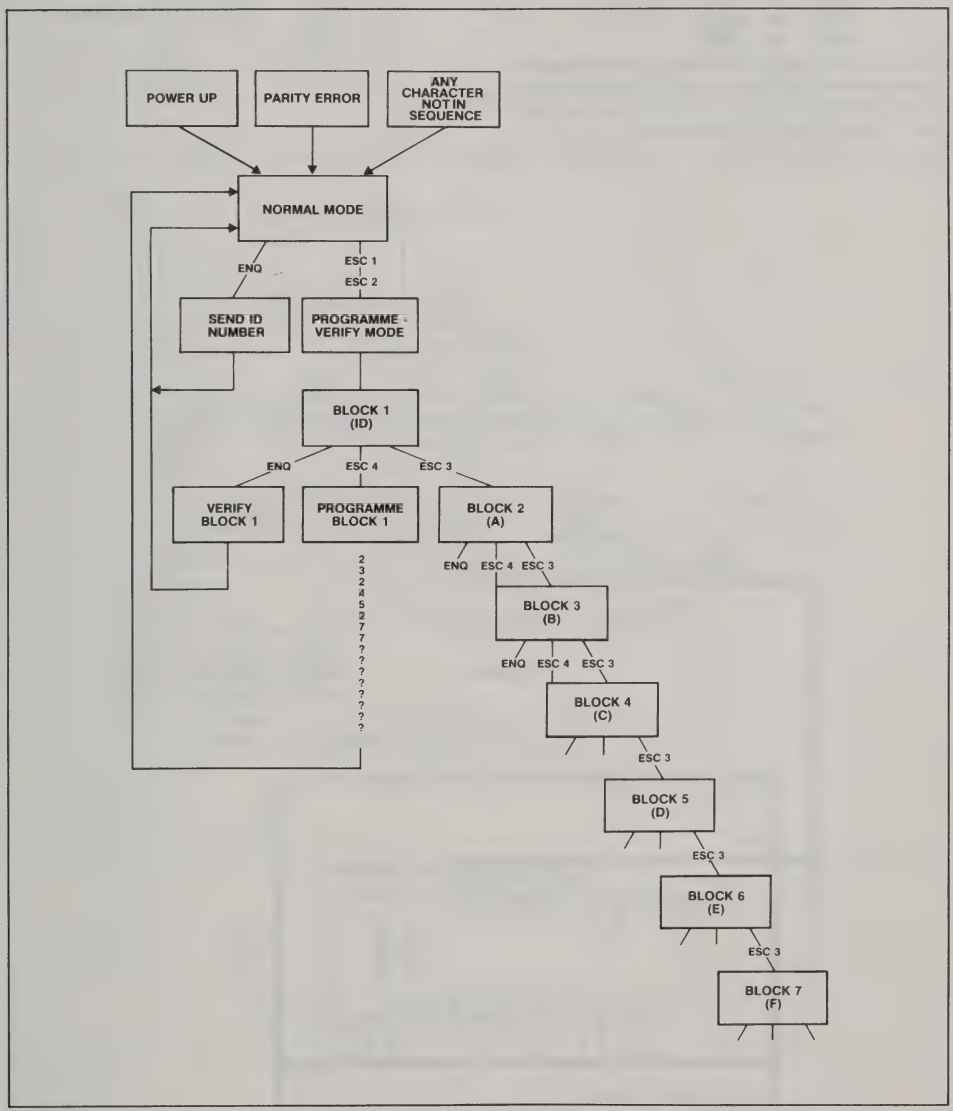


Fig.3 Flow diagram for programming ID and telephone numbers

APPLICATION

The Autodialler/Terminal Identifier has been designed for easy incorporation into the basic Teleview system. Special care has been taken to ensure that pin connections allow an easy and logical printed circuit layout.

The circuit diagram of the main electronics is shown in Fig. 4 and that of the Line Interface in Fig. 5.

The system has the following power supply requirements:

+ 9.1V	@	13mA	
+ 5V	@	140mA	(Relays)
+ 5V	@	55mA	(Logic)
−26V	@	8mA	

It may be acceptable to eliminate RLC and substitute two silicon diodes back to back across the modem side of the isolation transformer. This will be subject to approval by the British Telecom if used in Prestel equipment.

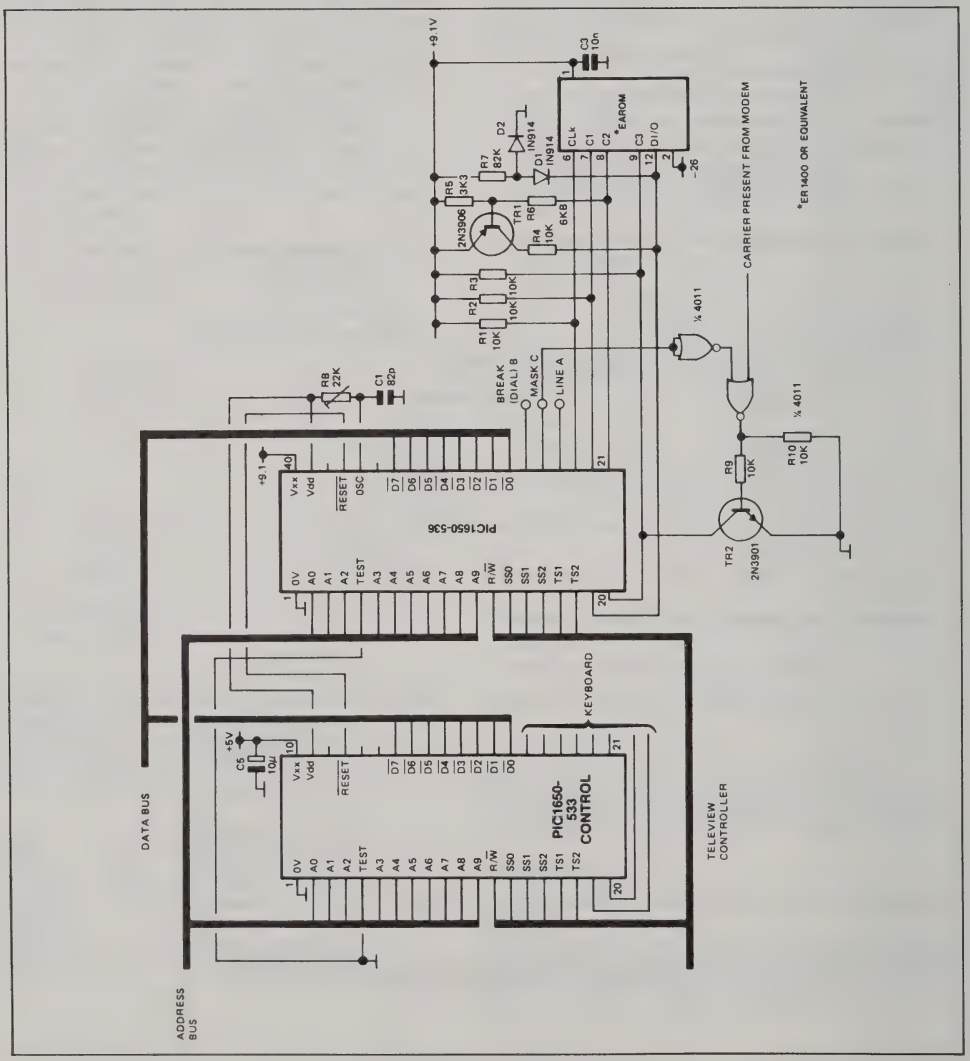
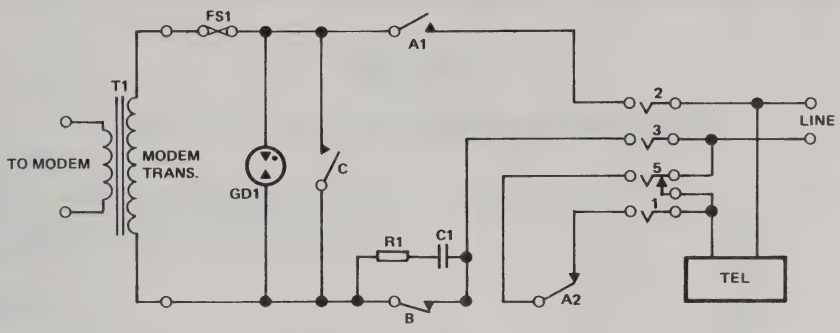
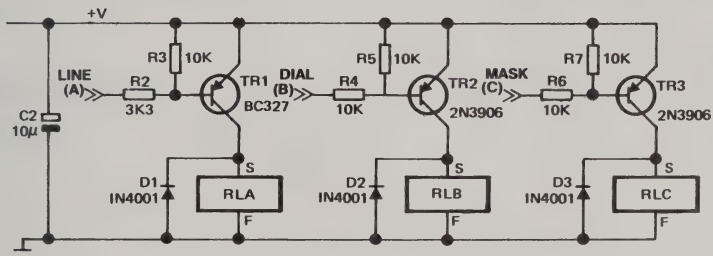


Fig.4 Auto dialler add on circuit for Teleview





T1	
RLA	CLARE CUP-V 10301
RLB	CLARE CUP-V 10201
RLC	CLARE CUP-V 10001
GD1	CERBERUS UC 90Ω
R1	100 ohms
FS1	250mA quick blow, ES4265
C1	2μF

Fig.5 Teleview line switching

PLESSEY
Semiconductors

SL471

BCD TO 1 OF 10 DECODER/VARICAP DRIVER

The SL471 can be used to decode the outputs of any of the ML920 series Remote Control Receivers. A 33V power supply voltage rating makes the circuits particularly useful for varicap driving in TV receivers.

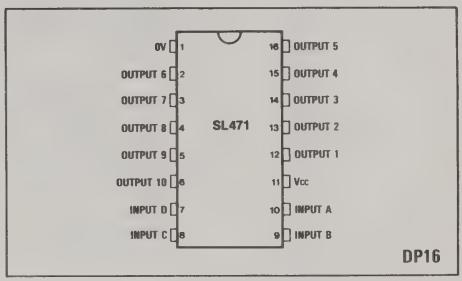


Fig.1 Pin connections - top view

FEATURES

- Up to 10 Programs
- Direct Drive From ML920 Series Receivers
- Direct Varicap Voltage Selection
- TTL Compatible Inputs
- Temperature Compensated Outputs
- Sufficient Output Current Available to Drive LED Indicators

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-55° C to +125° C
Operating temperature	-10° C to +65° C
Supply voltage	36V
Output current	20mA

D	C	B	A	O/P (HIGH)
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

Table 1 Positive logic decode table

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25° C; V_{CC} = 33V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage V_{CC}	11	30		36	V	
Supply current	11		3	5	mA	Output unloaded
Selected output level	2-6,12-16		V_{CC}-1.7	V_{CC}-2.5	V	100k load to 0V
			V_{CC}-2.5	V_{CC}-3	V	20mA output current
Unselected output	2-6,12-16			1	V	100k load to 0V
Input high state	7-10	1.7		20	V	
Input low state	7-10	-0.3		+0.4	V	
Input current V_{in} = 20V	7-10	0.8		1.4	mA	See input circuit Fig.3
Temperature coefficient of output voltage	2-6,12-16		-1.7		mV/° C	100k load to 0V

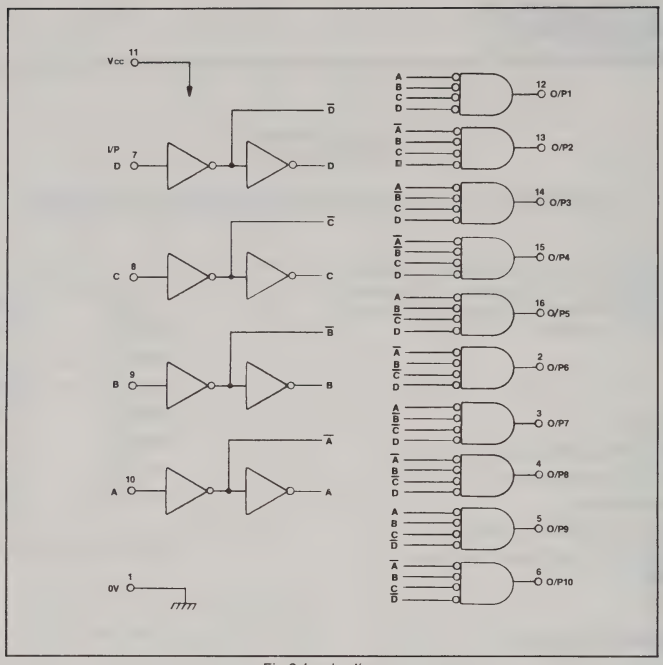


Fig.2 Logic diagram

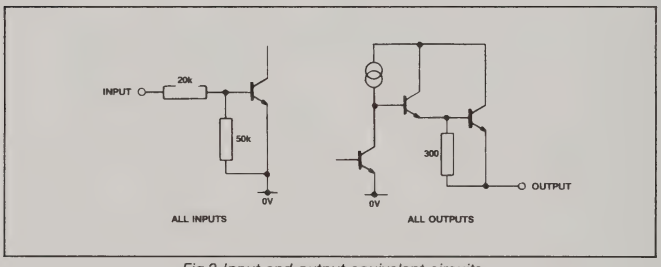


Fig.3 Input and output equivalent circuits

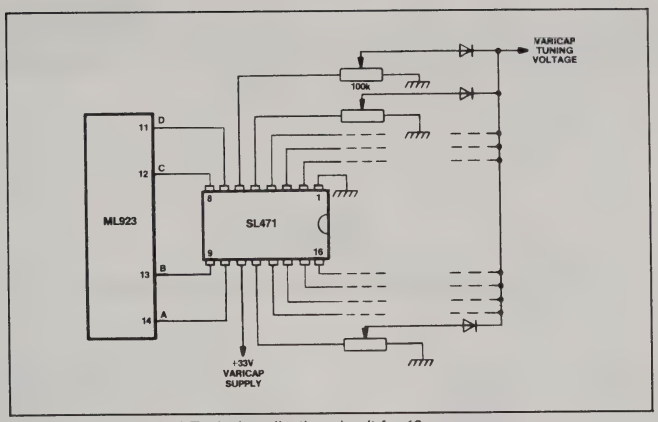


Fig.4 Typical application circuit for 10 programmes

PLESSEY
Semiconductors

SL486

INFRA RED REMOTE CONTROL PREAMPLIFIER

The SL486 is a high gain preamplifier designed to form an interface between an infra-red receiving diode and the digital input of remote control receiving circuits. The device contains two other circuit elements, one to provide a stretched output pulse facility and a voltage regulator to allow operation from a wide range of supplies.

FEATURES

- Fast Acting AGC Improves Operation in Noisy Environments
- Differential Inputs Reduce Noise Pick-up and Improve Stability
- Gyrator Circuit Allows Operation in Environments with High Brightness Background Light Levels
- Output Pulse Stretcher for use with Microprocessor Decoders
- On-Chip Stabiliser Allows Operation with a Wide Range of Supply Voltages
- Direct Interface to Plessey ML920 Series Remote Control Receivers
- Low Noise Output

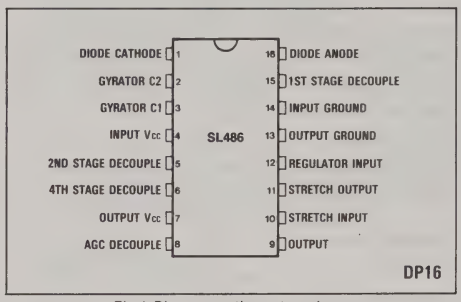


Fig.1 Pin connections top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V Pins 4 & 7)	+10V wrt V Pins 13 & 14
Regulator input voltage (V Pin 12)	-20V wrt V Pin 7
Output current	5mA
Stretch output current	5mA
Operating temperature range	0°C to +70°C
Storage temperature	-55°C to +125°C

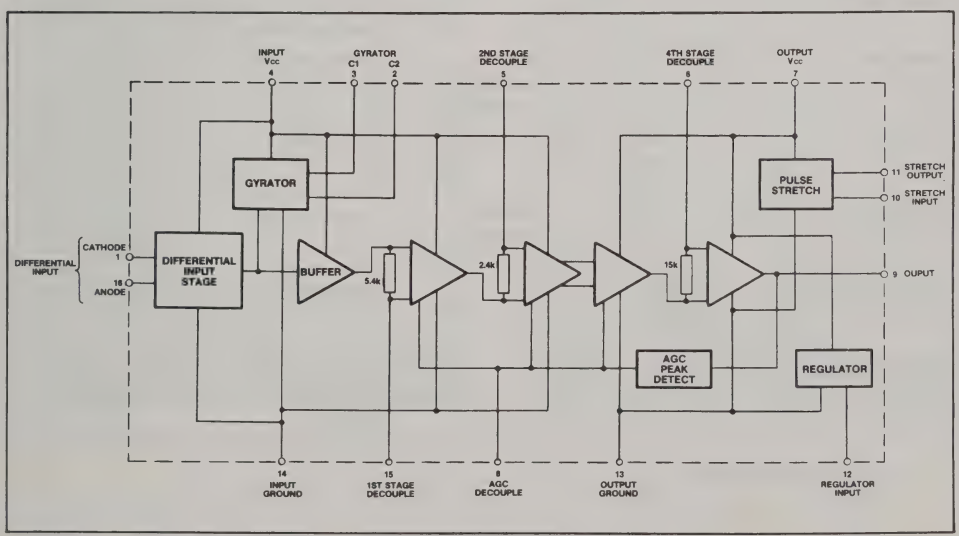


Fig.2 SL486 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25° C, V_{CC} = 4.5V to 7.0V

Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply current (See Note 1)	4,7		6.5	9.0	mA	V_{CC} = 5.0V, I_{DIODE} = 1.0μA } Pins 13 & 14 ground
	4	3.5+3xI_D	4.2+3xI_D	5+3xI_D	mA	V_{CC} = 4.5V, I_{DIODE} ≤ 1.5mA } ground
	4,7		8.5	10	mA	V_{CC} = 18V, I_{DIODE} = 1.0μA Pin 12 ground
Low voltage supply (external)	4,7(+ve), 13,14(-ve)	4.5		9.5	V	Input and output V_{CC} commoned, input and output ground commoned
High voltage supply (external)	4,7(+ve), 12(-ve)	8.4		18.0	V	Input and output V_{CC} commoned, input and output ground at internal regulated voltage
Internal regulated voltage	13(wrt 7)	5.9	6.2	6.5	-V	V Pin 7(+) to V Pin 12(-) = +16V
Voltage between input and output V_{CC}	4,7			1.5	V	At room temperature
				1.1	V	At 70° C
Minimum sensitivity of differential input	1,16	9.0		2.3	nA	I_{DIODE} = 1.0μA
		74.0		18.5	nA	I_{DIODE} = 100μA
		168.0		42.0	nA	I_{DIODE} = 0.5mA
Common mode rejection	1,16		35.0		dB	
Maximum signal input	1,16	3.0	4.0		mA(peak)	
AGC range			68.0		dB	
Output and stretch output pull-up resistance (internal)	9,11		55.0		kΩ	At 25° C
Stretch output pulse width (T_P)	11		2.4		ms	Capacitance Pin 9 to Pin 10 = 10nF; $T_P \simeq -Rx\,C \ln \left\{\frac{1.5}{V_{CC}}\right\}$,
T co-efficient on Rx			0.7		%/° C	Where Rx = 200kΩ ± 25 % (internal resistance)
Output low	9			Output ground +0.35	V	0.2mA Sink, max.
Output high	9	Output V_{CC} -0.5			V	5μA Source
Stretch output low	11			Output ground +0.5	V	1.6mA Sink, max.
Stretch output high	11	Output V_{CC} -0.1			V	Output open circuit 5μA Source
Supply rejection, input V_{CC}	4		1.5		V(peak)	Ripple amplitude at 100Hz, Pin 12 ground
			0.8		V(peak)	Ripple amplitude at 100Hz, Pins 13 & 14 ground

NOTE
1. I_D = I_{DIODE} = IR diode forward current

APPLICATION NOTES - REFER TO FIGURE 4

Diode Anode and Cathode (Pins 1 and 16) The infra-red receiving diode is connected between pins 1 and 16. The input circuit is configured so as to reject signals common to both pins. This improves the stability of the device, and greatly reduces the sensitivity to radiated electrical noise. The diode is reverse biased by a nominal 0.65V.

Gyrator C2 and C1 (Pins 2 and 3) The decoupling, provided by gyrator C2 and C1, rolls off the gain of the feedback loop which balances the DC component of the infra-red diode current. The values of C2 and C1 are chosen to produce a low frequency cut-off characteristic below a nominal 2kHz. Hence, the gyrator produces approximately 20dB rejection at 100Hz.

The gyrator consists of two feedback loops operating in tandem. Only one feedback path is functional when the DC component of the diode current is less than 200μA. This loop is decoupled by gyrator C2. For diode currents between 200μA and 1.5mA the second control loop is operative, and this is decoupled by gyrator C1.

The decoupling capacitors, gyrator C2 and C1, must be connected between pins 2 and 3, to pin 4. The series impedance of C2 and C1 should be kept to a minimum.

First Stage Decouple (Pin 15) The capacitor on pin 15 decouples the signal from the non-inverting input of the first difference amplifier (see also Figure 2). The capacitance of 15nF is chosen to produce a 2kHz low frequency roll-off.

The capacitor must be connected between pins 15 and 14 (the input ground).

Second Stage Decouple (Pin 5) The capacitor on pin 5 decouples the signal from the non-inverting input of the second difference amplifier. The capacitance of 33nF is chosen to produce a 2kHz low frequency roll-off. The capacitor must be connected between pins 5 and 4 (the input V_{CC}).

Fourth Stage Decouple (Pin 6) The capacitor on pin 6 decouples the signal from the non-inverting input of the fourth difference amplifier. The capacitance of 4.7nF is chosen to produce a 2kHz low frequency roll-off. The capacitor must be connected between pins 6 and 7 (the output V_{CC}).

AGC Decouple/Delay Adjust (Pin 8) The output of the fourth difference amplifier is followed by a peak detector, which is used to provide an AGC control level. This produces a current source which is limited to 10mA at pin 8. The AGC decouple capacitor (C5 normally 150nF) filters the pulsed input, and the resultant level controls the gain of the first three difference amplifiers.

The AGC control level exhibits a fast attack/slow decay characteristic. Immediately infra-red pulses are detected, the gain will be reduced, so that any weaker noise pulses that are also received will not be seen at the output. Thus, provided the infra-red pulses are the most intense, it is possible to receive data in noisy environments. The slow decay keeps the AGC level intact during data reception, and produces a delay before any received noise may become present at the output, when transmission ceases.

Output (Pin 9) The output will be low, pulsing high with a source impedance of a nominal 55kΩ, for a received infra-red pulse. It is a linear amplification of the input and swings between output ground and output V_{CC}.

Stretch Input and Stretch Output (Pins 10 and 11) A typical infra-red PPM system transmits very narrow pulses. The duration of these pulses is typically 15μs, so in order to utilise a microprocessor based decoder system it is necessary to lengthen the received pulse. This stretched output can be obtained from pin 11 when a capacitor is connected between pins 9 and 10.

The width of the pulse is determined by the value of this coupling capacitor (C8 in Figure 3) and is given by:

$$T_p = -R_x C_8 \ln \left\{ \frac{1.5}{(V_4 - V_{13})} \right\}$$

where T_p = pulse width in ms
R_x = 200kΩ (see electrical characteristics)
C_8 = coupling capacitance
and $(V_4 - V_{13})$ = potential between input V_{CC} and ground (pins 13 and 14)

The stretch output is normally high pulsing low for a received infra-red pulse, and swings between output V_{CC} and output ground.

Regulator Input (Pin 12) The device can be operated with supplies of between 4.5V and 9.0V connected between input/output ground (pins 14 and 13) and input and output V_{CC} (pins 4 and 7) as shown in Figure 3.

The device can be operated with supplies in excess of 9.0V by utilising the on-chip regulator. In this case connections are made between output V_{CC} (pin 7) and the regulator input (pin 12) as shown in Figure 4. A supply voltage of between 9.0V and 18V will then cause the output ground to be regulated at a level nominally 6.4V below the output V_{CC} (pin 7).

The regulator will, however, lose control with a potential difference of less than 9.0V. Below this level the voltage on pin 13 will track nominally 1.5V above the level of pin 12.

When the regulator is not used (low voltage operation), pin 12 must be shorted to output ground (pin 13).

OPERATING NOTES - REFER TO FIGURES 3 AND 4

Gyrator C1 (Pin 3) If the environment in which the device is operating, limits the background light such that the DC component of the diode current has a maximum of 200μA, it may be desirable to omit (see Figure 3) the more bulky and costly 68μF capacitor, gyrator C1 shown in Figure 4. In this case pin 3 can be left open circuit. The resultant application will then have a characteristic of greatly reduced gain when the ambient light causes the DC current to rise above this threshold.

The 68μF capacitor can alternatively be replaced by a resistor. The outcome of this is to further reduce the gain in ambient light levels above the 200μA threshold. Below this threshold the overall gain is slightly enhanced as the light level approaches the threshold value. If chosen this resistance should lie between 10kΩ and 200kΩ.

Noise Immunity The stretch output can also be used as a means of improving performance relating to a receiver system, over and above its main purpose of providing a stretched output facility. Including C8 (Figure 4) causes the output pulses (from pin 9) to be subjected to the stretch input threshold. Thus any noise pulses from pin 9 that are below this threshold will not be seen at the stretch output (pin 11).

A further improvement can be made, utilising this stretch input threshold by including some additional filtering of the output (C10 in Figure 4). This can be adjusted in value (typically 100pF) to reduce some of the noise pulses that otherwise cross the threshold, to a level below the threshold.

It must be noted that the stretch output logic sense is inverse (for microprocessor applications) from that of the output (pin 9), and the cost of re-inversion may be deemed uneconomical for the improvements gained.

Screening Use of screening for the device, and associated components, improves the performance and immunity to externally radiated noise. The screening method used must protect the sensitive front-end of the device; provided that

the diode, pin 1, pin 16, C2 (pin 2) and the first stage decouple (pin 15) are screened, it may be found that for the application considered, the remaining circuitry need not be so protected.

In applications where externally radiated noise is minimal, it may be possible to reduce any screening to pins 1 and 16, and the diode connections, only. In some instances, no screening may be necessary, but this largely depends on the level of radiated noise, the decoupling/filtering employed and the receivers decoding technique.

Decoupling Typical decoupling arrangements for use with or without the regulator, are given in Figures 4 and 3 respectively. When using the regulator, further improvements in high frequency supply rejection are possible by the inclusion of R2. The value can be chosen so as to keep the pin 12 end of R2 within the -9.0 to -18V (w.r.t. pin 7) specified voltage range. For example if using the 920 series remote control receivers, on a supply of 16V, a typical value for R2 would be 200Ω.

Note that the regulator is a low impedance point between pins 12 and 13. C7 thus maintains a low impedance path between pins 4 and 12 at high frequencies.

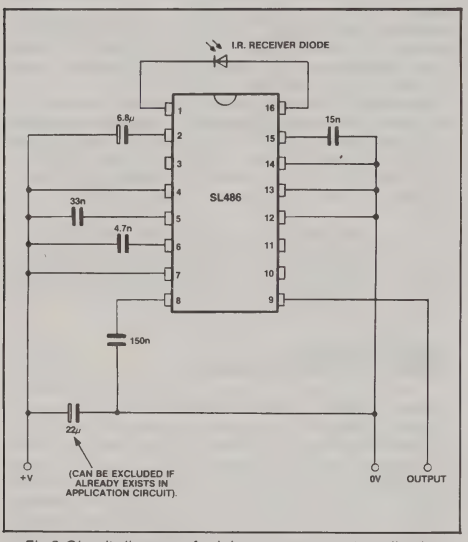


Fig.3 Circuit diagram of minimum component application (showing low voltage operation)

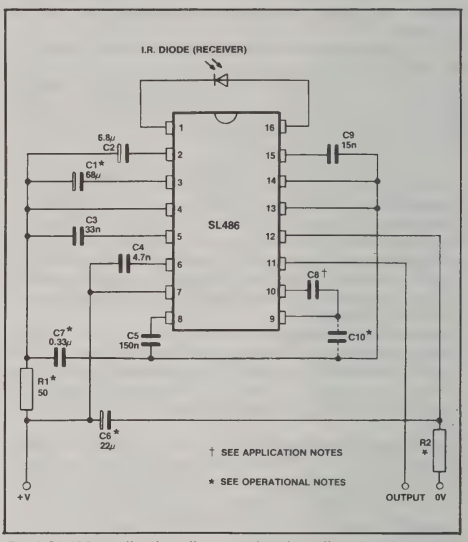


Fig.4 SL486 application diagram showing all optional circuitry (Note: Supply decoupling and connections for use of voltage regulator; also pulse stretched output)

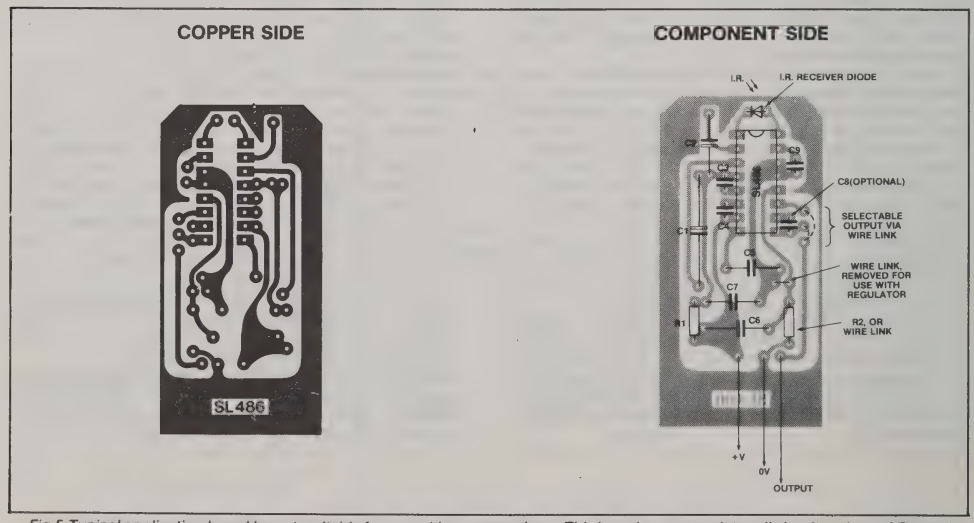


Fig.5 Typical application board layout; suitable for use with a screened can. This board accommodates all circuit options of Figure 4 (except C10).

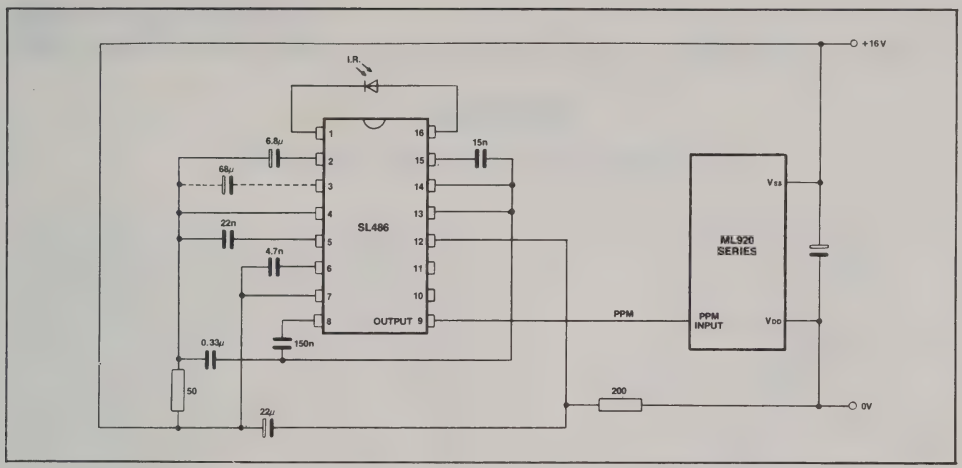


Fig.6 Application diagram for use with ML920 series remote control receivers, utilising on-chip supply stabiliser

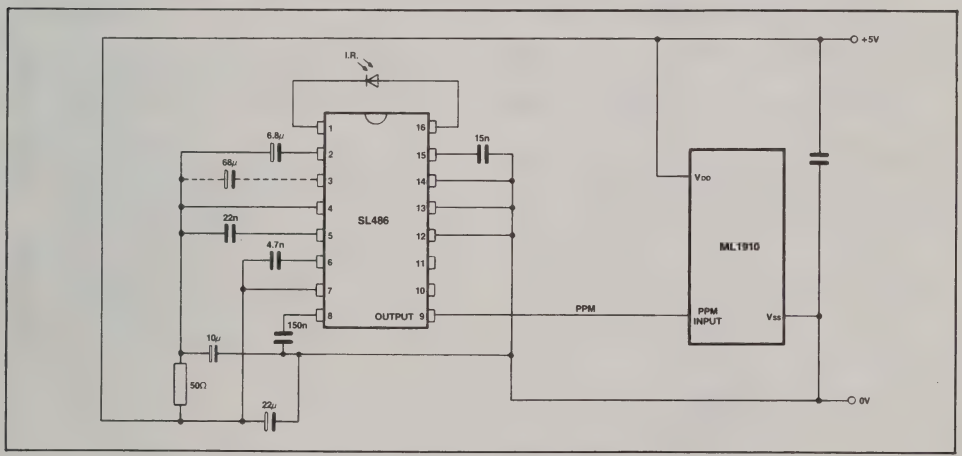


Fig.7 Circuit diagram of interface with ML1910 remote control receiver

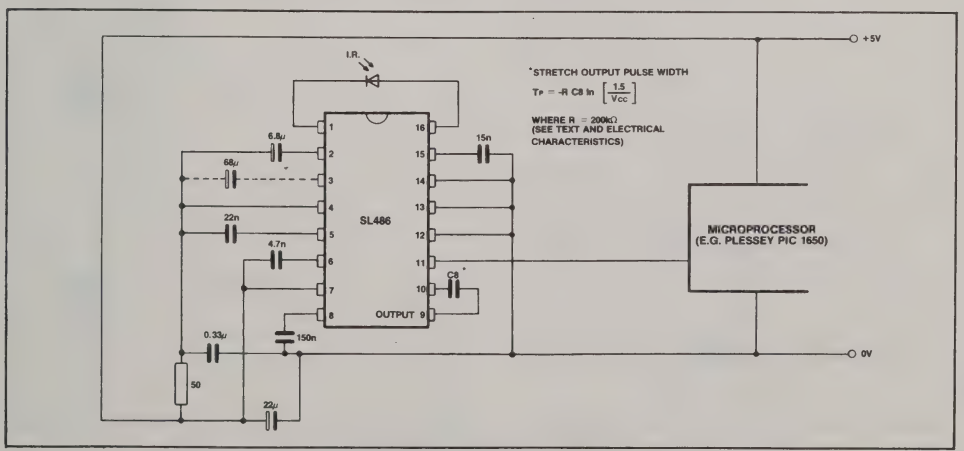


Fig.8 Circuit diagram of microprocessor interface, utilising on-chip pulse stretching facility

PLESSEY
Semiconductors

SL490B

REMOTE CONTROL TRANSMITTER

Plessey Semiconductors have developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra red transmission, cable, radio or telephone links may also be utilised. Pulse position modulation (PPM) is used with or without carrier and automatic error detection is also incorporated. Although initially designed with TV remote control in mind the devices may equally easily be applied for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The SL490B is an easily extendable, 32 command, pulse position modulation transmitter drawing neglible standby current. It may be used with the ML920 series of remote control receivers.

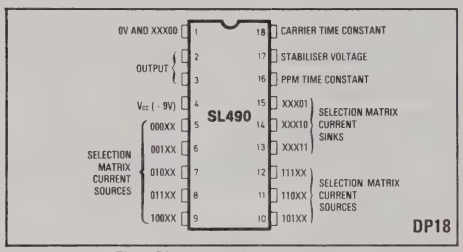


Fig.1 Pin connections - top view

FEATURES

- Ultrasonic or Infra-red Transmission
- Direct Drive for Ultransonic Transducer
- Direct Drive of Visible LED When Using Infra-red
- Very Low Power Requirements
- Pulse Position Modulation Gives Excellent Immunity From Noise and Multipath Reflections
- Single Pole Key Matrix
- Switch Resistance Up To 1kΩ Tolerated
- Few External Components
- Anti-Bounce Circuitry On Chip

QUICK REFERENCE DATA

- Power Supply: 9V, Standby 6μA, Operating 8mA
- Modulation: Pulse Position With or Without Carrier
- Coding: 5 Bit Word Giving a Primary Command Set of 32 Commands
- Key Entry: 8 × 4 Single Pole Key Matrix
- Data Rate: Selectable 1 Bit/Sec to 10k Bit/Sec.
- Carrier Frequency: Selectable 0Hz (no carrier) to 200kHz.

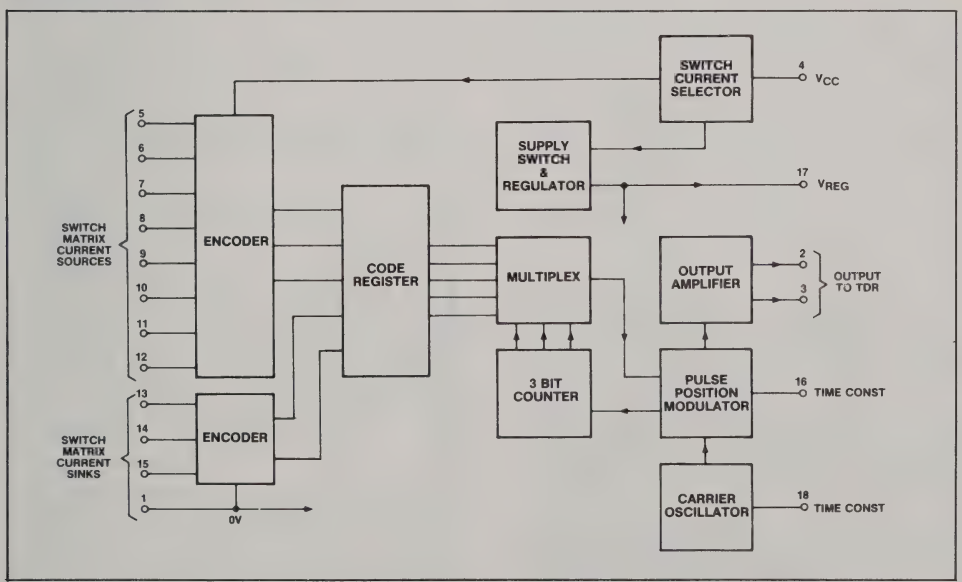


Fig.2 SL490B transmitter block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 25°C V_{CC} = +7V to +10.5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply current	4		9.5	16	mA	V_{CC} = 9.5V
Standby supply current	4			10	μA	
Stabilised voltage	17	4.1		4.9	V	
Output current available from stabilised supply	17			1	mA	
Output voltage swing	2,3	V_{CC} -1			V	Unloaded
Output voltage	2			1	V	I_2 = 10mA } Peak value < 1ms
Output voltage	3			1	V	I_3 = 5mA }
External switch resistance	5-15			5	kΩ	
External carrier resistor R2	18	20	40	80	kΩ	C2 = 680pF fc = 40kHz
t_1 deviation from calculated value	2,3			±10	%	R1 = 15k } t_1 = 0.95 C1 R1
using fixed timing components	2,3			±10	%	R1 = 60k } See Fig.4
PPM resistor	16	15	30	60	kΩ	
Variation of t_1 and t_0 with V_{CC}						
t_1 with V_{CC} = 7V/t_1 with V_{CC} = 10.5V	2,3			±4	%	
t_0 with V_{CC} = 7V/t_0 with V_{CC} = 10.5V	2,3			±4	%	
Ratio t_0/t_1	2,3	1.4		1.6		
Pulse width t_p	2,3	0.11 t_1		0.22 t_1		
Interword gap	2,3		3			The interword gap is 3 times t_1 derived by counting

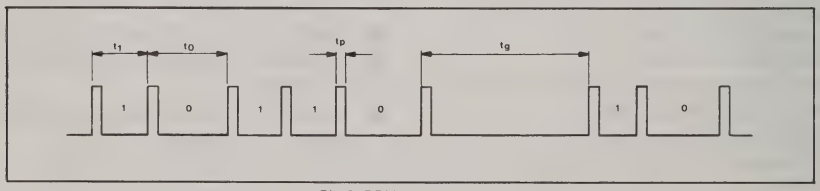


Fig.3 PPM word notation

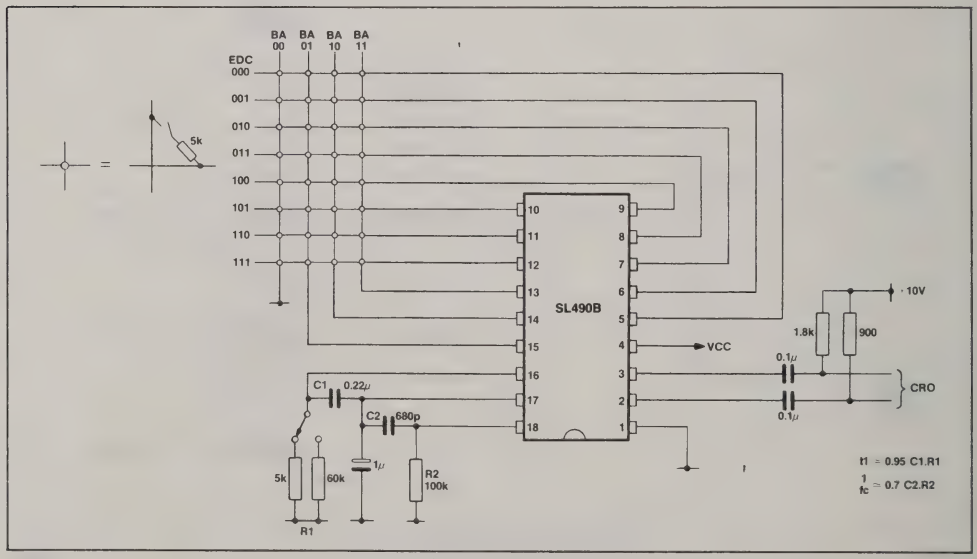


Fig.4 Test circuit

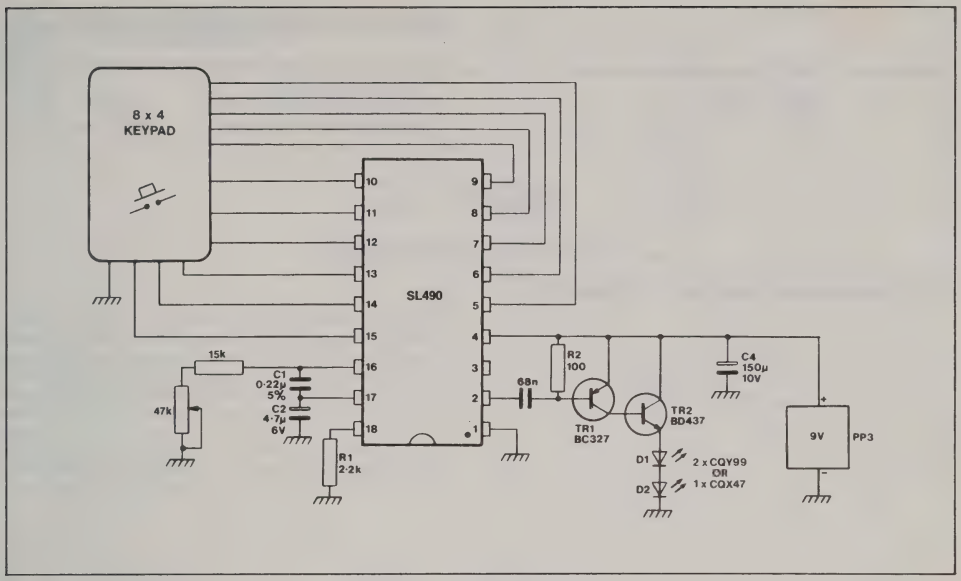


Fig.5 Infra-red application circuit

OPERATING NOTES

Fig.5 shows the circuit for a simple infra-red transmitter where the PPM output from pin 2 of the SL490B is fed to the base of the PNP transmitter TR1, producing an amplified current pulse about 15μsec wide. This pulse is further amplified by TR2 and applied to the infra-red diodes D1 and D2.

The current in the diodes and the infra-red output is controlled by the quantity, type, and connection method of the diodes and also by the gain at high currents of the transistors.

The most common solution where cost is important is to use 2 single-chip diodes, such as the CQY99 connected in series.

Improved output can be obtained by using four CQY99 diodes in a series parallel arrangement, but it is usually simpler to use 2 multichip diodes such as the CQX47 connected in parallel or a single CQX19 which gives similar results.

A significant increase in range can be obtained by using diodes such as the CQY99 in conjunction with a plated plastic parabolic reflector.

When building the transmitter, care should be taken with the choice of the capacitor C4 and with the circuit layout, particularly when multi-chip diodes are being used, as the current pulses can be as high as 6 to 8Amps.

Transistor choice is also important and any substitutes should have high current gain characteristics and switching speeds similar to those specified in Fig.3.

An increase in output can be obtained by connecting TR2 in common emitter configuration, but care should be taken not to exceed the rating of the diodes.

Choice of PPM Frequencies

Although the ML920 series of remote control receivers is designed to work over a wide range of PPM frequencies, the actual usable range may be restricted by the application. The analogue outputs on the ML920, ML922 and ML923 serve as a good example, since the outputs will step up or down, one step for each pair of PPM words received. This in turn fixes the rate of increment or decrement of the volume or colour controls of a TV set.

When the transmitter is being used with an infra-red link, with high current pulses fed to the diodes as in Fig.5, power consumption will increase with frequency. It is thus advisable that with a battery power supply, the slowest PPM rate consistent with adequate response time should be chosen.

Setting Up Procedure

When designing a remote control system using the SL490 in conjunction with the ML920 range of receiving circuits it is important from a manufacturing point of view for all transmitters to be interchangeable. The timing capacitor C1 should be chosen to give the required T1 time calculated from the formula $T1 = 1.4CR$ with $R \triangleq 33k$. The R value should be made up of a series potentiometer resistor combination with sufficient adjustment to compensate for the I.C. and component tolerances.

The timing components on the receiver can be selected using the formula

$$f_{RX} = \frac{1}{0.15CR} \pm 20\% \text{ where } f_{RX} = \frac{40}{t_o}$$

t_o being the PPM logic 0 time from the transmitter.

If the recommended value of potentiometer and fixed resistor, as shown in Fig.6, are used, then the value of R in the above formula should be 84kΩ. This gives the maximum frequency adjustment range, which is needed to cope with component and IC tolerances.

Final adjustment is made by setting the period on the receiver oscillator time constant pin to 1/40th of the transmitter PPM logic 0 time using the potentiometer. Connection to the receiver time constant pin should be made using a x10 oscilloscope probe to reduce circuit loading.

When adjusting the ML920, the monitor output can be used for setting up, but in this case, a figure of 1/20th of the transmitter PPM logic 0 time should be used as the monitor output is at half the oscillator frequency.

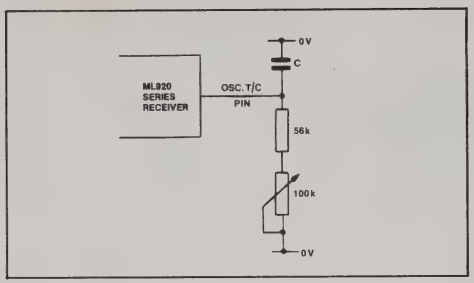


Fig.6 Recommended receiver time constant components

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7V to 9.5V
Total power dissipation	600mW
Operating temperature range	–10°C to +65°C
Storage temperature range	–55°C to +125°C

PLESSEY
Semiconductors

SL 1430

TV IF PREAMPLIFIER

The SL1430 is a fixed gain IF preamplifier for television with an output optimised for driving Plessey second generation low capacitance surface acoustic wave (SAW) filters. The addition of one external capacitor allows the amplifier to drive normal capacitance SAW filters from Plessey or from other manufacturers.

The device features on chip decoupling and differential output, requiring a minimal number of external components to be used.

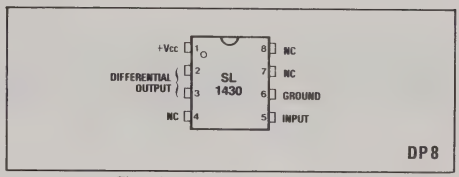


Fig.1 Pin connections - top view

FEATURES

- Low cost
- Low noise
- Low external component count
- Low distortion
- Direct 12V operation
- Can be used with different types of SAW filters

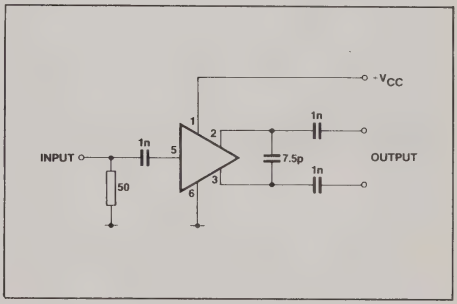


Fig. 2 Test circuit

QUICK REFERENCE DATA

- 22dB gain at 40MHz
- 12V supply at 25mA
- 120mV rms. input handling

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C
Supply voltage = +12V
Frequency = 40MHz
Output load = 7.5 pF (Pins 2 and 3)
Measurements made using test circuit Fig. 2.

Characteristic	Pin	Value Min	Value Typ	Value Max	Units	Conditions
Supply voltage	1	7	12	13.5	V	
Quescent current	1	22	33	40	mA	Pins 2, 3O/C
Cut-off frequency (–3dB)	5, 2/3	60	110		MHz	
Voltage gain		18	22	26	dB	
Input signal for 46dB intermodulation	5		120		mV	Red colour bar
Input signal for 1% crossmodulation	5		75		mV	(wanted level 20mV unwanted modulation 65%)
Input signal for 1dB sync tip compression	5	130			mV	rms.
Noise figure	5		4		dB	
Input impedance	5		300Ω// 4.2pF			

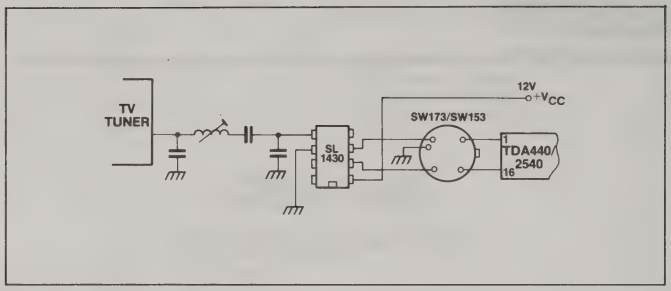


Fig. 3 Typical applications

SL1430 TYPICAL CHARACTERISTICS AT ,12V, +25°C, WITH SW173 AS LOAD (7.5pF) (FIGS. 5 TO 10) Unwanted signal with 65% amplitude modulation at 10KHz

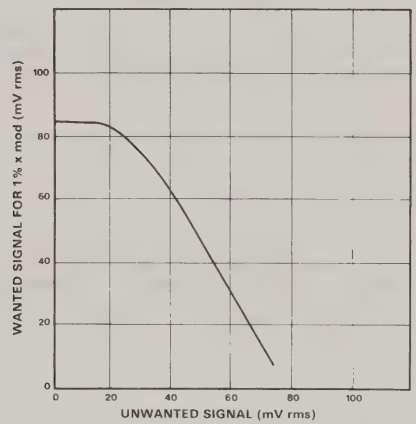


Fig. 4 Cross modulation performance (see note 1)

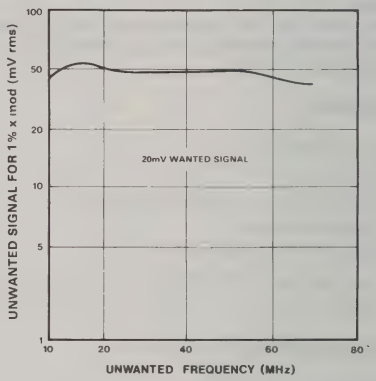


Fig. 6 Cross modulation performance V frequency of unwanted signal (see note 1)

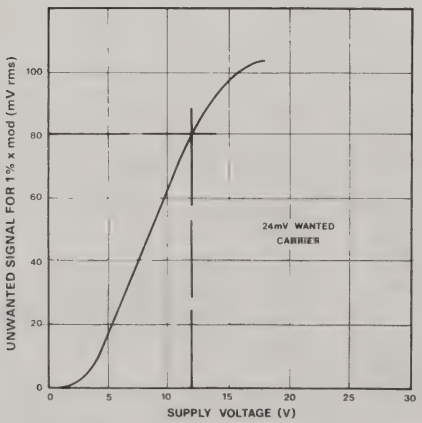


Fig. 5 Cross modulation performance V supply voltage (see note 1)

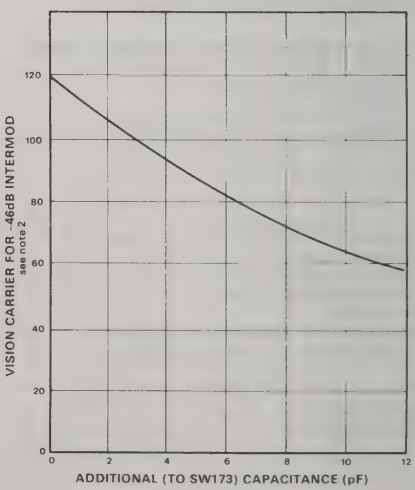


Fig. 7 Intermodulation performance v. load capacitance

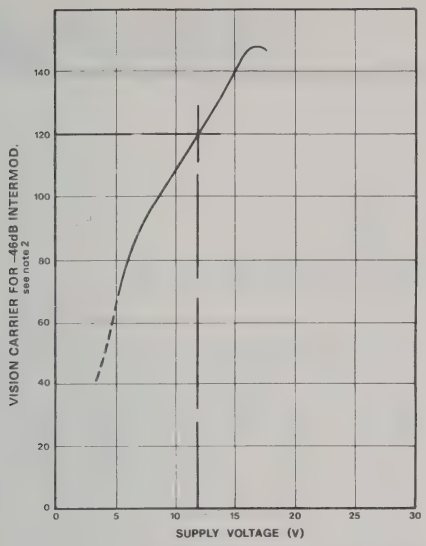


Fig. 8 Intermodulation performance v. supply voltage

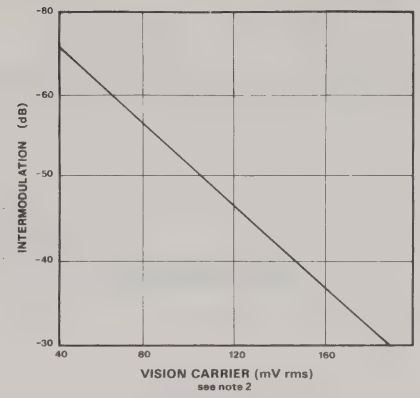


Fig. 9 Intermodulation performance (see note 2)

NOTE 1. Signal level refers to peak rms. i.e. The effective sync. tip level of a composite video signal.

NOTE 2. The test signal employed corresponds to the red bar of a transmitted colour bar and consists of the following elements related to the sync. tip level, the vision carrier at 38.9MHz–6dB, the colour carrier at 34.5MHz–18dB, and the sound carrier at 33.4MHz–7dB.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	—0.5V to +25V
Operating temperature range	—10°C to +65°C
Storage temperature range	—55°C to +125°C

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Semiconductors

SL1431/2

TV IF PREAMPLIFIERS WITH AGC GENERATOR

The SL1431 and SL1432 are fixed gain IF preamplifiers for television with a differential output optimised for driving Plessey surface acoustic wave (SAW) filters. Besides providing the necessary gain block between the tuner and SAW filter they also supply a properly derived, broadband AGC signal to the tuner, the SL1431 providing the correct sense signal for a NPN tuner, and the SL1432 for an PNP tuner. The tuner AGC threshold is internally preset to a value to allow adequate signal handling in the SL1431 and SL1432 and does not normally require any external adjustment. However, to account for the large variations in signal handling capability which is encountered on some tuners, the tuner AGC threshold may be externally adjusted by altering the bias on pin 1.

Both devices feature on-chip decoupling for a minimum external component count.

AGC Signal

For high input signal levels the voltage on pin 7 goes low with SL1431 and high with the SL1432.

QUICK REFERENCE DATA

- 23dB Gain at 40MHz
- 12V Supply at 25mA
- 120mV R.M.S. Input Handling
- 15mA Tuner AGC Capability

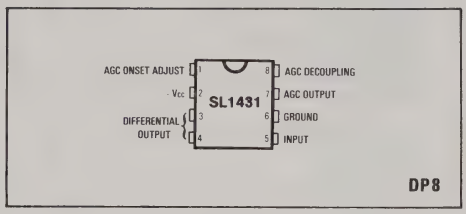

Fig.1 Pin connections - top view

FEATURES

- Properly Derived Tuner AGC
- Low Cost
- Low Noise
- Low External Component Count
- Low Distortion
- Direct 12V Operation
- Can be used with Different Types of SAW Filters

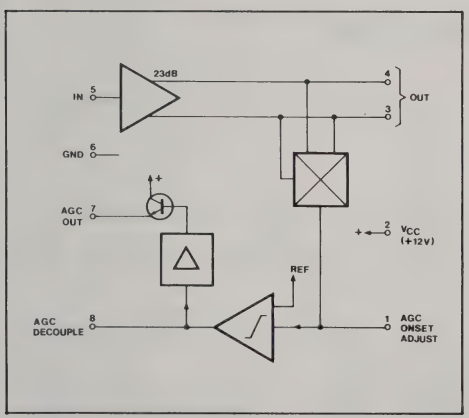

Fig. 2 Block diagram

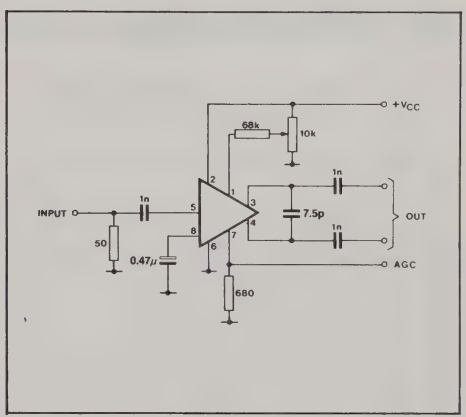

Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C
Supply voltage = +12V
Frequency = 40MHz
Output load = 7.5pF (Pins 3 and 4)
Measurements made using test circuit Fig. 3.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply Voltage	2	7	12	13.5	V	
Quiescent Current	2	22	33	40	mA	Pins o/c
Cut-off frequency (—3dB)	5	60	110		MHz	
Voltage gain		20	23	26	dB	
Input signal for 46dB intermodulation	5		120		mV	Red colour bar
Input signal for 1% cross-modulation	5		75		mV	(wanted level 20mV, unwanted modulation 65%)
Input signal for 1dB sync tip compression	5	130			mVrms	
Noise figure	5		4		dB	
Input impedance	5		300Ω //4.2pF			
Tuner AGC						
Output current	7	15	20		mA	@ 10.0 V
Input impedance	1		6		kΩ	

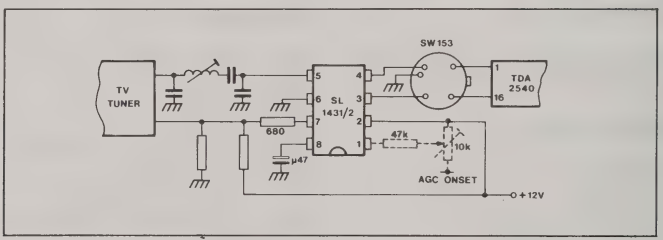

Fig. 4 Typical applications

SL1431 TYPICAL CHARACTERISTICS AT 12V, +25°C, WITH SW173 AS LOAD (7.5pF) (FIGS. 5 TO 10) Unwanted signal with 65% amplitude modulation at 10kHz

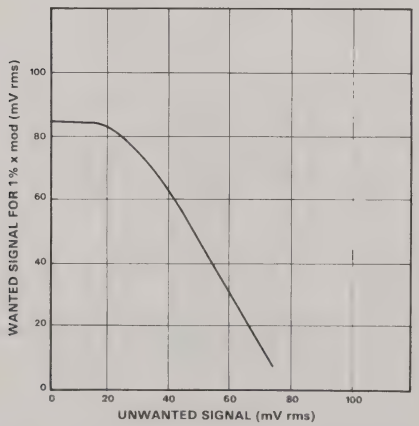

Fig. 5 Cross modulation performance (see note 1)

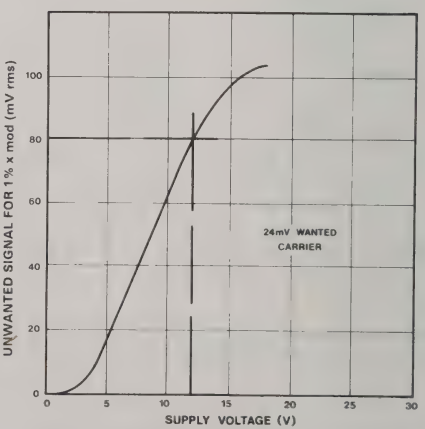

Fig. 6 Cross modulation performance V supply voltage (see note 1)

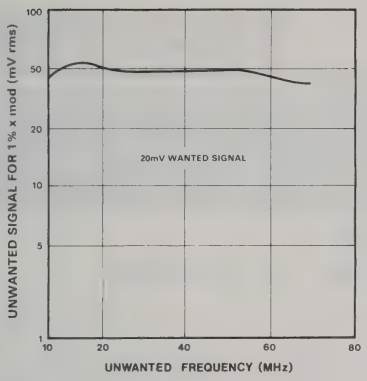

Fig. 7 Cross modulation performance V frequency of unwanted signal (see note 1)

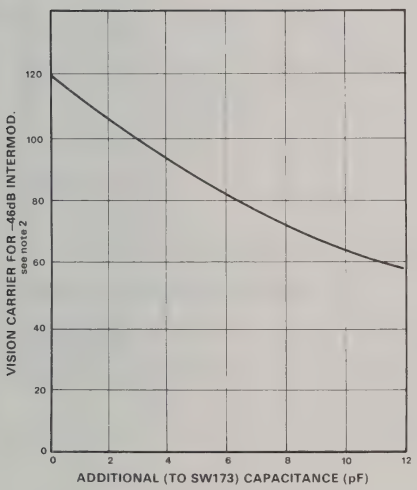

Fig. 8 Intermodulation performance v. load capacitance

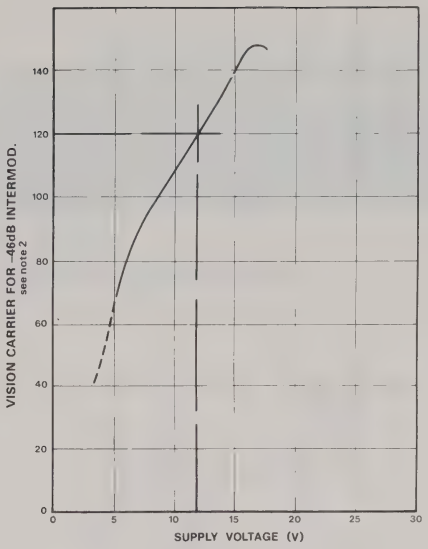

Fig. 9 Intermodulation performance v. supply voltage

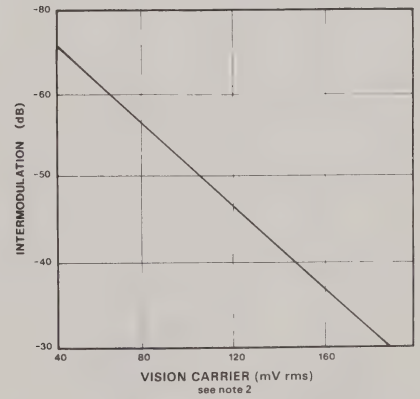

Fig. 10 Intermodulation performance (see note 2)

NOTE 1. Signal level refers to peak rms. i.e. The effective sync. tip level of a composite video signal.

NOTE 2. The test signal employed corresponds to the red bar of a transmitted colour bar and consists of the following elements related to the sync. tip level, the vision carrier at 38.9MHz–6dB, the colour carrier at 34.5MHz–18dB, and the sound carrier at 33.4MHz–7dB.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	—0.5V to +25V
Operating temperature range	—10°C to +65°C
Storage temperature range	—55°C to +125°C

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SL1451 EXP

WIDEBAND PLL FM DETECTOR FOR SATELLITE TV

The SL1451 EXP is a phase locked loop demodulator for use in wideband FM systems. It is intended for use with an IF input frequency from 300MHz to 650MHz in satellite receivers. It consists of an input RF amplifier, signal level detector, UHF phase detector, UHF oscillator and video/loop amplifier. Both positive and negative going video outputs are available.

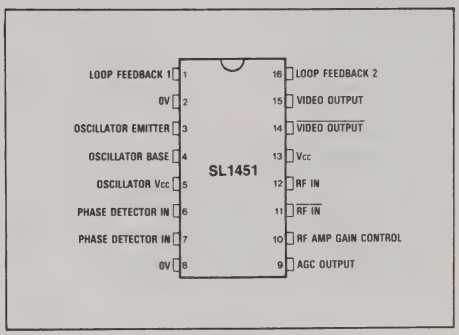

Fig.1 Pin connections - top view

FEATURES

- Complete PLL System for Wideband FM Demodulator
- 8dB Noise Threshold Performance Typical
- Low External Component Count
- Positive and Negative Going Video Output Available

APPLICATIONS

- DBS Receivers
- Wideband Data Communications Demodulation

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**0° C to 70° C**
Supply voltage	11V
Storage temperature range	-55° C to 125° C
Junction temperature	+175° C

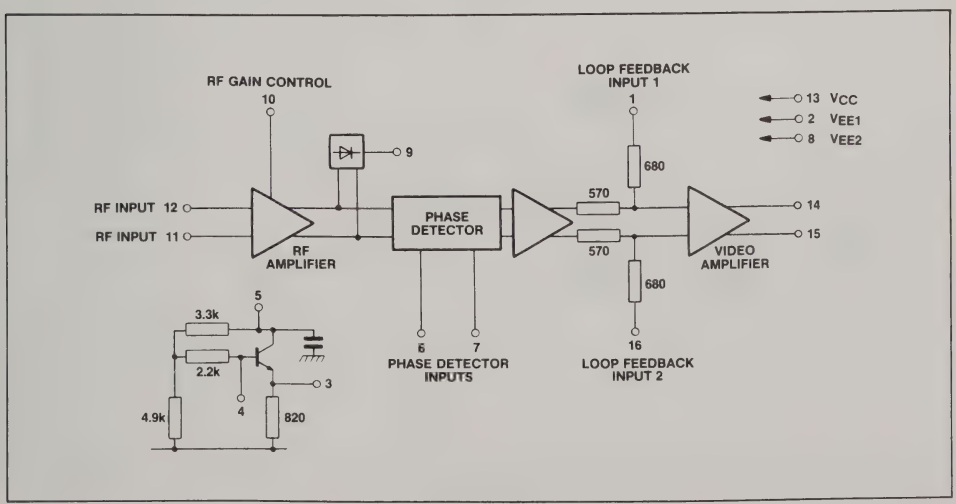

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C V_{CC} = 7.4V to 9V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	13,5	40	55	65	mA	
Supply voltage	13,15	7.4	8.2	9	V	
Minimum oscillator frequency			300		MHz	
Maximum oscillator frequency			700		MHz	
Phase detector input level						
from oscillator	6,7	-15	-10	-5	dBm	
RF input level	11,12	-25	-15	-5	dBm	
Phase detector gain			0.5		V/Radian	
AGC output	9		300		μA	No input signal
			140		μA	-20dBm input signal
Oscillator lock range			50		MHz	See Note 1
VCO slope			14		MHz/V	
Video output voltage	14,15		1		Vt pk to pk	14MHz pk to pk deviation
Intermodulation products			-40		dBm	See Note 2
Video bandwidth			18		MHz	

NOTES
1. All characteristics from oscillator lock range to video bandwidth are determined by the application circuit. These results were gained with the circuit in Fig.3.
2. Signal 1 4.433MHz Deviation = 13.5MHz pk-pk
   Signal 2 6MHz Deviation =2MHz pk-pk

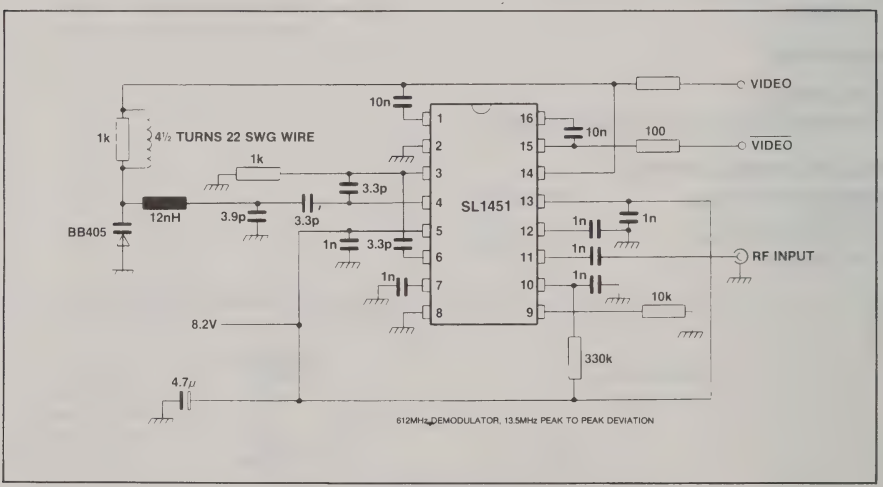

Fig.3 Typical application circuit

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SL1452

WIDEBAND LINEAR FM DETECTOR FOR SATELLITE TV

With a minimum of external components, the SL1452 forms a complete wideband FM detector suitable for use in satellite TV. The video output voltage and bandwidth may be optimised by adjustment of the working Q of the quadrature coil. The device features electrostatic protection on all pins.

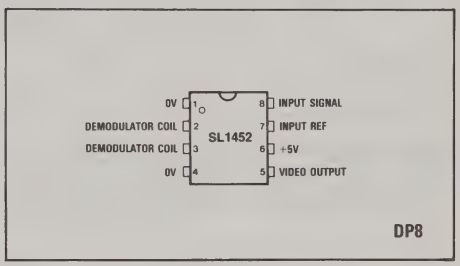

Fig.1 Pin connections - top view

FEATURES

- High Operating Frequency Simplifies Image Filtering
- Excellent Threshold
- Negligible Differential Gain and Phase Errors
- Video Bandwidth Suitable for High Definition TV
- High Sensitivity and Wide Dynamic Range
- Wide operating frequency range 300 to 1000MHz

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10°C to +80°C**
Storage temperature	-55°C to +125°C
Supply voltage Pin 6	7V
Input voltage Pin 7 or 8	2.5V p-p
Junction temperature	+175°C

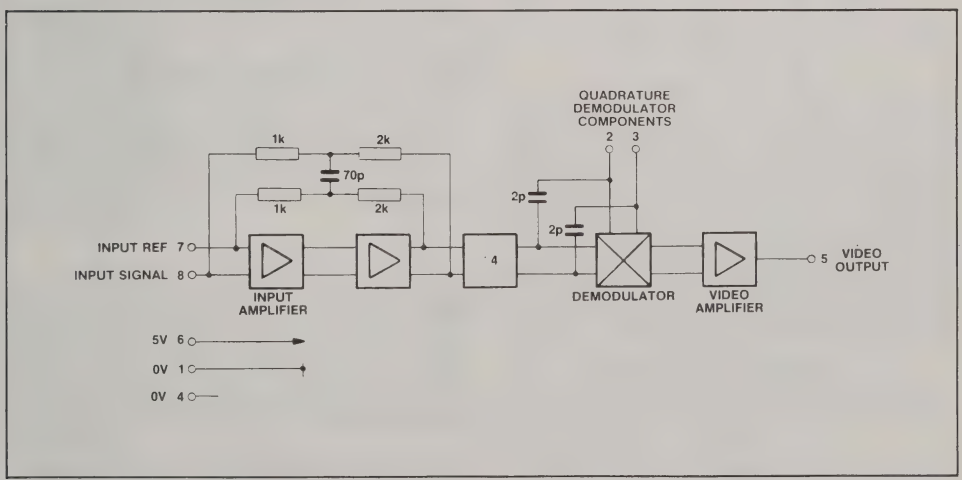

Fig.2 SL1452 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; V_{CC} = +4.5V to +5.5V; Q = 6 f = 612MHz

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current I_C	6		40	50	mA	V_{CC} = 5V
Video output voltage	5		0.7		V p-p	Δf = 13.5MHz p-p
Video bandwidth	5		14		MHz	
Minimum operating frequency	8		300		MHz	
Maximum operating frequency	8		1000		MHz	
Input sensitivity	8		5	10	mV rms	
Input overload	8	0.3	0.7		V rms	
Intermodulation	5		-60		dB	product of input modulation f = 4.4MHz Δf = 13.5MHz p-p and f = 6MHz Δf = 2MHz p-p (PAL colour and sound subcarriers)
Differential gain	5		<±1%			Δf = 13.5MHz p-p. Demodulated staircase referred to input staircase before modulation
Differential phase	5		<±1		deg	demodulated colour bar waveform referred to waveform before modulation
Signal to noise ratio	5	70			dB	ratio of output with Δf = 13.5MHz p-p at 1MHz to output rms noise in 10MHz bandwidth with Δf = 0

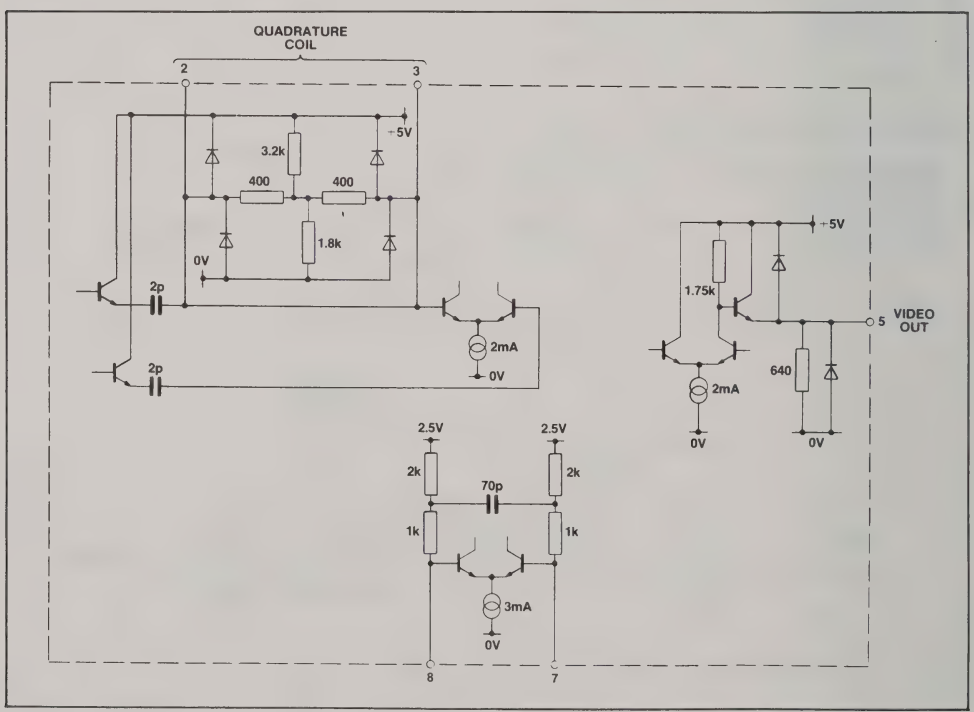

Fig.3 Input/output interface circuits

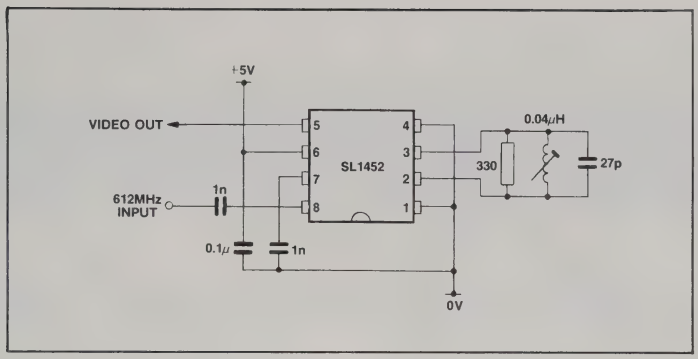

Fig.4 Typical application

APPLICATION NOTES

The SL1452 FM demodulator has a very simple application with very low external component count. This is demonstrated by the applications circuit diagram fig.4, but as with most integrated circuits, particularly those working at high frequencies some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be ensured by the simple precaution of keeping all components close to the SL1452, maintaining short lead lengths and ensuring a good low impedance earth plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies: multilayer ceramic types usually providing small size and adequate high frequency performance. For the quadrature coil tuning capacitor a fairly stable component should be selected to prevent excessive drift. The power supply decoupling capacitor from pin 6 to ground should be 0.1μF minimum but the input coupling and decoupling values can be smaller, about 330pF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if maximum performance is to be obtained.

First determine the quadrature circuit operating frequency which is a quarter of the input frequency on pin 8 due to the two internal divide by 2 circuits (see fig.2).

Choose suitable values for L and C to resonate at the correct frequency using:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The value of C should be greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive level to the demodulator and thereby restrict the video output available. In general for operation in the 400 to 600MHz range, an inductance value between 40 and 60 nano Henrys is recommended.

Once suitable L and C values have been determined, the working Q for the quadrature circuit should be set, the Q value determining the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from table 1 and the graphs in fig.5.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800-ohm resistor between pins 2 and 3 must be taken into account when calculating R.

Example

Design a quadrature circuit to demodulate a carrier with centre frequency 480MHz and video bandwidth of 10MHz.

Choose L = 0.04μH
then C = 43.98pF (nearest preferred value 47pF)
from table 1 Q required is approximately 6
therefore total R required is:

$$R = Q2\pi fL$$

$$= 6 \times 2 \times \pi \times \frac{480}{4} \times 10^6 \times 0.04 \times 10^{-6}$$

$$= 181 \text{ ohms}$$

allowing for the internal 800 ohm resistance, the external resistance required is 234 ohms. Choose 270 ohms.

It should be remembered that the internal 800 ohm resistance is subject to a fairly wide production tolerance and if fairly close control of video bandwidth is required, the L and C ratio may require some adjustment to ensure that the external R is sufficiently low to swamp the effect of internal resistance changes. The value of 270 ohms obtained in the example is low enough to allow adequate control.

In order to overcome the effects of component tolerances, it will usually be necessary to make either the L or C a variable component, the value being adjusted to obtain best linearity.

Q	BANDWIDTH
10	7.5MHz
6	14MHz
4	23MHz

Table 1

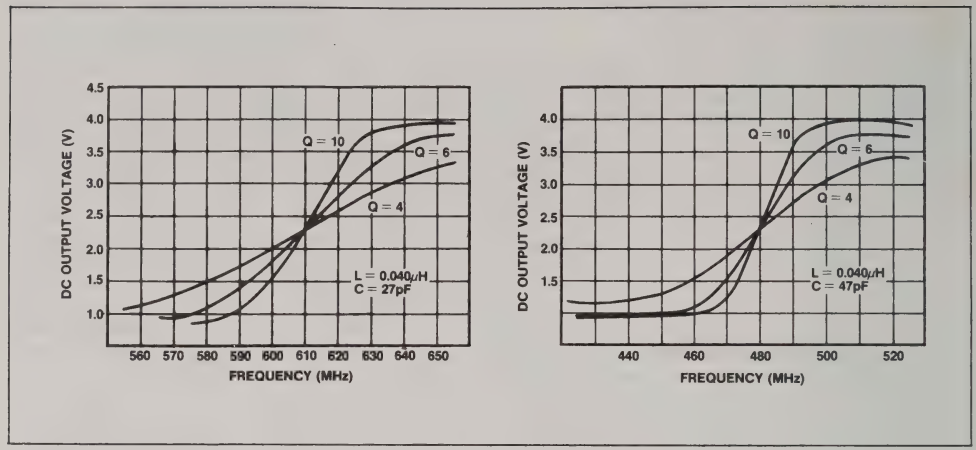

Fig.5 Output voltage versus input frequency

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SL9100 EXP

VIDEOTEXT DATA SLICER AND CLOCK REGENERATOR

The SL9100 has been designed to recover data from composite video type signals, e.g. Teletext broadcasts. As well as retrieving data, the SL9100 will resynchronise a Clock output to the Data stream and also provide a composite sync output.

FEATURES

- Slicing Of Data Adapts To Both The Black And White Video Levels
- Pre-Adaption Of The White Level Occurs At The Beginning Of Each Video Line
- Pre-Adaption Avoids Slicing Of The Colour Burst Signal
- TTL Compatible Data Output
- TTL Compatible Resynchronised Clock Output
- TTL Compatible Composite Sync Output
- Interfaces Directly To The Plessey Teleview System, Specifically The MR9710 And MR9735

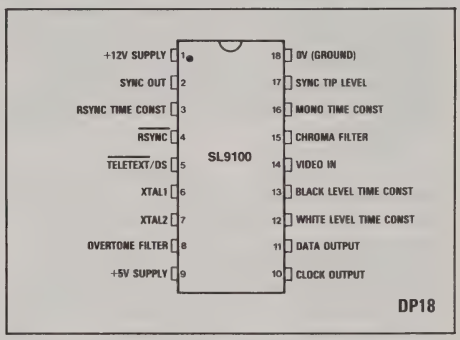

Fig.1 Pin connection - top view

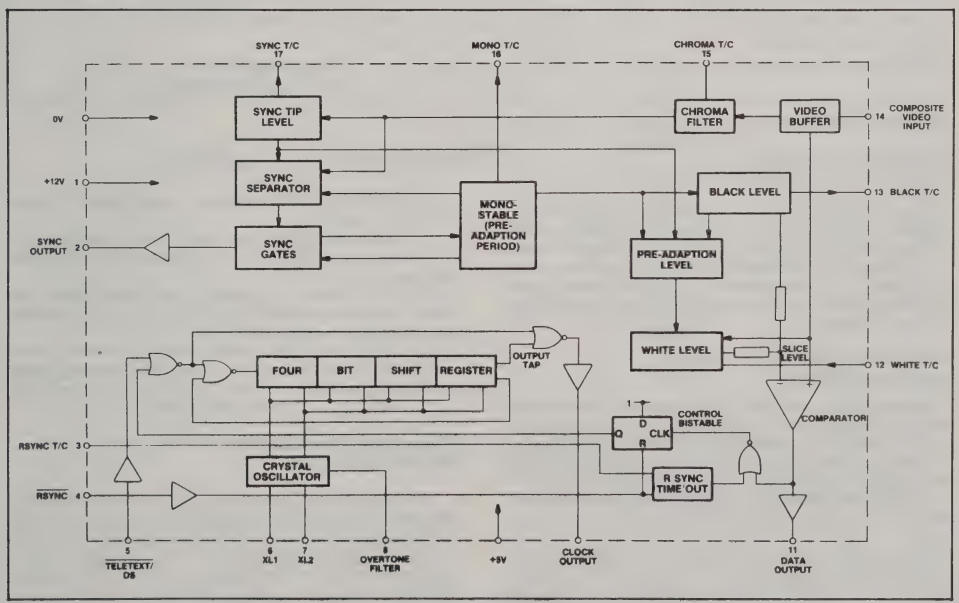

Fig.2 SL9100 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): $T_{amb} = 25°C$

Characteristic	Pin No. (Symbol)	Value			Unit	Conditions
		Min.	Typ.	Max.		
5V supply voltage	9	4.2		5.8	V	
5V supply current	9		44		mA	5V rail = 5V
12V supply voltage	1	10.8		13.2	V	
12V supply current	1		11		mA	12V rail = 12V
Video input (p-p)	14	1.5		4.5	V	AC coupled, positive video
Input impedance	14		10		kΩ	
Signal/noise ratio	14	20			dB	W.R.T. data height, during data line, with band limited white noise
Co-channel interference	14		130		mV(pk)	26.042kHz sine wave added to video
Co-channel interference	14		130		mV(pk)	52.083kHz sine wave added to video
$\overline{\text{RSYNC}}$ input pull-up	4	3.0			kΩ	Internal to +5V
$\overline{\text{RSYNC}}$ input low level	4			0.5	V	0.5mA max. source
$\overline{\text{RSYNC}}$ input high level	4	4.8			V	20μA max. source from pin
$\overline{\text{RSYNC}}$ input capacitance	4			5	pF	
$\overline{\text{Teletext}}$/DS pull-up	5		10		kΩ	Internal to +5V
$\overline{\text{Teletext}}$/DS input low	5			0.5	V	500μA max. source
Sync output low level	2			0.4	V	
Sync output high level	2	3.5			V	
Data output low level	11			0.4	V	Sink 1.5mA min. } Drive
Data output high level	11	3.0			V	Source 1.5mA min. } 25pF max.
Clock output low level	10			0.4	V	Sink 1.5mA min. } Drive
Clock output high level	10	3.5			V	Source 1.5mA min. } 25pF max.
Black level source	13		25		μA	
White level sink	12		25		μA	
Mono source	16		50		μA	
Sync tip level source	17		20		μA	
Pre-adaption	12	60		100	%	Over video input range
Data slice level	(11)		50		%	Over video input range
Sink slice level	(14)		150		mV	Level above sync tips at pin 14
Crystal oscillator frequency (fx)	6/7		55.5		MHz	Components as in Fig.5
Clock output frequency	10	1.5	fx/8	7.5	MHz	Free running (no video input)
Data output frequency	11	1.5		7.5	MHz	
Regenerated clock phase	10	60		90	ns	Trailing edge lag w.r.t. data output trailing edge

CIRCUIT DESCRIPTION

Video Input (Pin 14) And Chroma Time Constant (Pin 15)

The incoming video is AC-coupled into an emitter follower, biased to 6.4V through 10kΩ. This provides 'buffered video' which is then fed to an external pad through 1kΩ, where an external capacitor (C8 = 1nF) acts as a single pole filter. This filter subdues the chrominance signal, providing 'filtered video', after correcting for the voltage drop in the 1kΩ resistor.

Sync Time Constant (Pin 17) And Sync Output (Pin 2)

'Filtered video' is fed into a conventional negative peak detector using a current source into an external capacitor (C10 = 22nF). The output of this is modified in two ways:

1. With no signal present, it is clamped typically 0.2V below the quiescent video level, ensuring no SYNC output or
2. With SYNC detected the output will represent a SYNC slice level typically 0.15V above the SYNC tips (positive video).

This provides slicing of 'filtered video' which produces positive SYNC's at ECL levels for internal use. This signal is then inverted in a TTL output buffer, producing negative going composite SYNC.

Monostable Time Constant (Pin 16)

This provides the 'pre-adaption period' which has the following functions:

1. To determine when pre-adaption takes place and
2. Clamp a capacitor to the black level for subsequent reference.

The monostable is triggered on the trailing SYNC edge with a typical period of 4μs. This is set by an external capacitor (C9 = 100pF) on pin 16.

The associated SYNC gates ensure that slicing of the colour burst, or other noise immediately following SYNC, does not give rise to a false SYNC pulse or pre-adpation period. Fig.3 shows the resultant action.

Black Level Time Constant (Pin 13) And Pre-Adaption Level

The black level circuit comprises two separate peak detectors. The first tracks negative excursions of DATA in the video signal, while the positive detector resets the black level during the pre-adaption period. The positive detector is normally gated out. The negative peak detector includes a current source which charges the external black level time constant capacitor (C6 = 2.2nF) on pin 13.

During the pre-adaption period, a fixed gain amplifier is enabled to produce a 'pre-adaption level'.

A voltage proportional to the SYNC height w.r.t. black level is added to the black level and fed to the white level circuitry (i.e. estimated data size).

White Level Time Constant (Pin 12) And Data Output (Pin 11)

The white level is determined by a positive peak detector which stores either the most positive data level, or estimated data level (pre-adaption). The white level time constant is determined by an external capacitor (C5 = 2.2nF, pin 12) which is drained by an internal current sink.

The mean value of both black and white levels is chosen to be the slice level at which DATA is recovered from the video signal. This mean level is normally set at 50% of the difference of black and white levels as indicated by the two resistors shown in Fig.2. The DATA, at ECL levels, is used for Clock regeneration and also feeds a TTL buffer for output at pin 11.

Crystal Oscillator (Pins 6 And 7) And Overtone Filter (Pin 8)

The crystal oscillator uses a third overtone crystal and a parallel tuned circuit (pin 8) to ensure oscillation at 55.5MHz. It provides two anti-phase clocks for driving an on-chip four-bit shift register.

Clock Output (Pin 10) And $\overline{\text{Teletext}}$/DS (Pin 5)

The crystal oscillator output is divided by eight by the 4-bit shift register to provide a 7MHz (typ.) clock from incoming data. The output of the control bistable provides synchronisation of the regenerated clock to the recovered data.

When the control bistable output and $\overline{\text{Teletext}}$/DS pin are both low, the shift register will fill with zeros. Note that DS is grounded for Teletext operation, and that an $\overline{\text{RSYNC}}$ pulse will reset the control bistable output to zero. The output of the first NOR gate associated with the register will hold the clock output to zero until a negative transition of Data clocks the control bistable. This NOR gate output will then go low, allowing the zeros in the register to be clocked out as ones, and also fed back to the input and re-loaded as ones. This provides resynchronisation, and the output tap on the shift register is such that the negative clock edge occurs during the middle of each Data bit to provide correct clock phase w.r.t. recovered data.

Note that if the $\overline{\text{Teletext}}$/DS pin is held high, the clock output is a free-running division of the 55.5MHz oscillator.

$\overline{\text{RSYNC}}$ Input (Pin 4) And $\overline{\text{RSYNC}}$ Time Constant (Pin 3)

Clock resynchronisation takes place at the start of each line. An $\overline{\text{RSYNC}}$ pulse will occur at the beginning of each possible Teletext line. If data is present, the clock is re-started, checked for frequency by the Teleview system and a second $\overline{\text{RSYNC}}$ pulse occurs to provide final resynchronisation (see Timing Diagram, Fig.4). If, on a possible Teletext line, no data is present then the $\overline{\text{RSYNC}}$ time-out circuit provides re-start of the clock before the end of the line (typically 20μs after the last $\overline{\text{RSYNC}}$ pulse). This uses an external capacitor (C1 = 1nF) on pin 3, pulled up through a 20kΩ resistor, which is discharged by each $\overline{\text{RSYNC}}$ pulse.

APPLICATION NOTES

Black And White Time Constants

The black and white time constants are set by the external capacitors, C6 and C5 respectively, and the internal source and sink currents of 25μA, on pins 13 and 12. The values of C6 and C5 can be calculated once the rate at which the levels must change, in order to accommodate signal level fluctuations, has been pre-determined.

For the white level, an additional restriction must be taken into account in order to avoid false data to be sliced. This level must not fall to that of the black level, within a line period, or it will be similar to the quiescent black level, and hence the data slice level also. In order to be safe, this means that the value of C5 should not be less than 2.2nF.

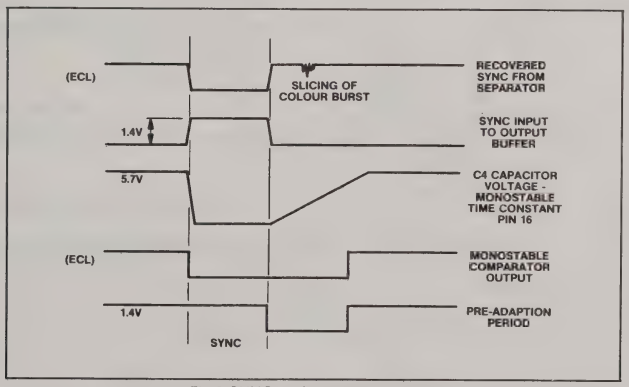

Fig.3 SYNC and monostable timing

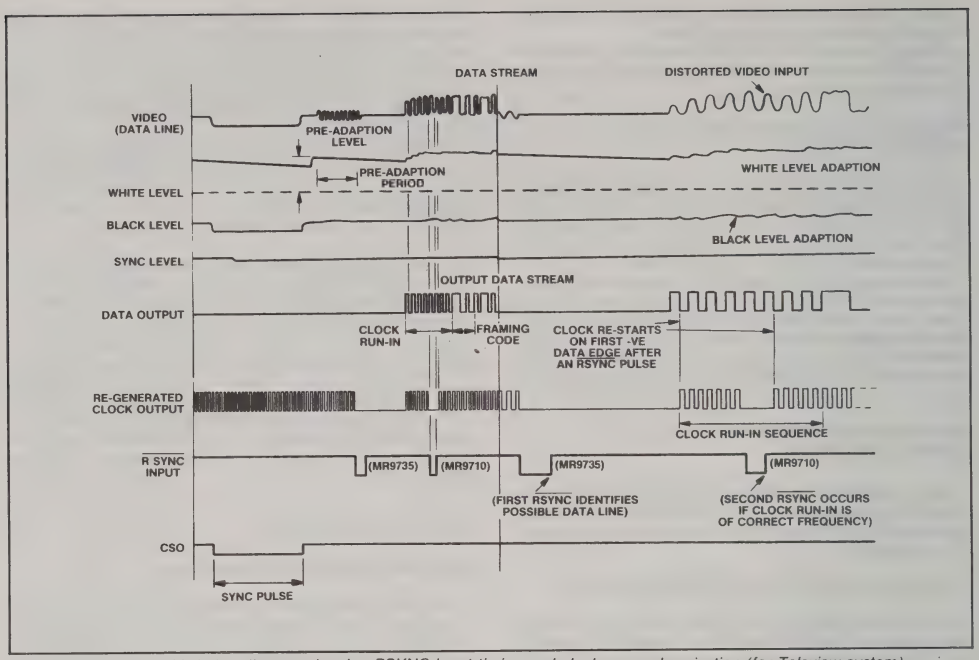

Fig.4 SL9100 timing diagram showing RSYNC input timing and clock re-synchronisation (for Teleview system)

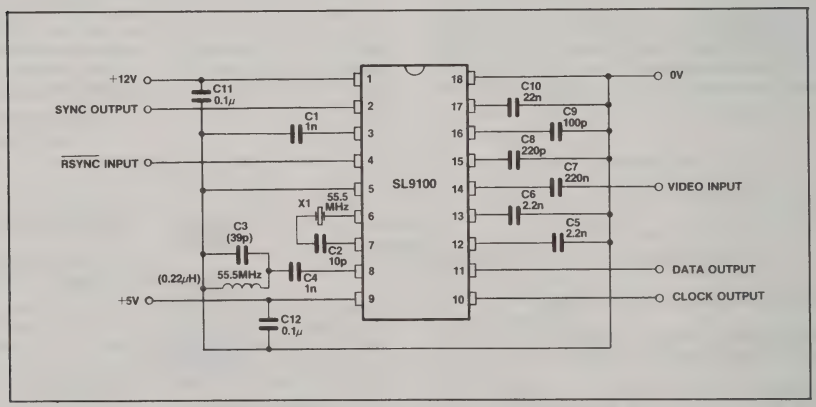

Fig.5 Application circuit showing external components

PLESSEY
Semiconductors

SP4541

1 GHz ÷ 256

The SP4541 is one of the range of Plessey Consumer high speed dividers.

The device is intended for use in television frequency synthesis systems. It has a division ratio of 256 with a single TTL output and incorporates an on-chip preamplifier with a differential input. The input pins may be used as UHF and VHF, with only a slight loss of sensitivity, if suitable drive circuitry is employed.

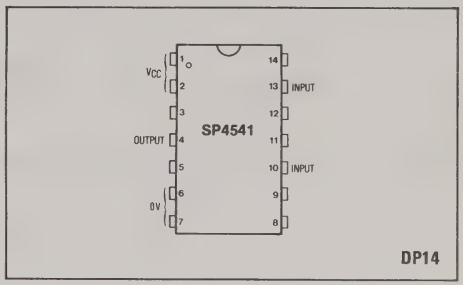

Fig.1 Pin connections - top view

FEATURES

- On-chip wideband amplifier
- High input sensitivity
- High input impedance
- Low output radiation
- TTL output

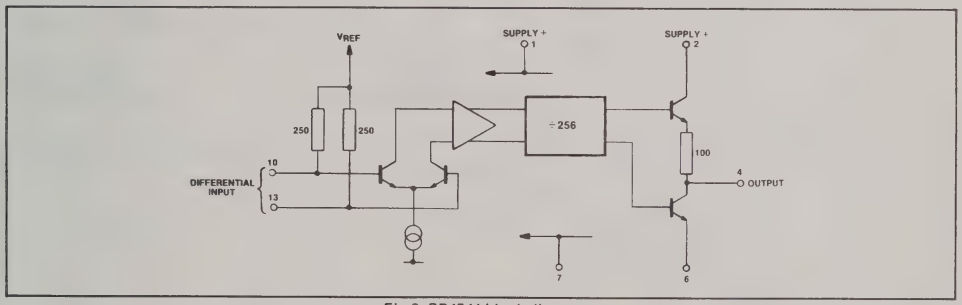

Fig.2 SP4541 block diagram

ELECTRICAL CHARACTERISTICS (see Fig.3)

Test Conditions (unless otherwise stated):
T_{amb} = 0°C to +65°C, V_{CC} = +5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	1, 2	4.5	5	5.5	V	
Supply current	1, 2		70	90	mA	
Input voltage, V_{IN}, 80MHz	10	17.5		200	mVrms	Sine wave into 50Ω
300MHz	10	17.5		200	mVrms	
500MHz	10	17.5		200	mVrms	
700MHz	10	17.5		200	mVrms	
1000MHz	10	17.5		200	mVrms	
Output voltage High		3.3			V	Sourcing 0.2mA
Low				0.4	V	Sinking 2mA

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7 V
Input voltage	2.5V p-p
Ambient operating temperature	-10°C to +65°C
Storage temperature	-55°C to +125°C

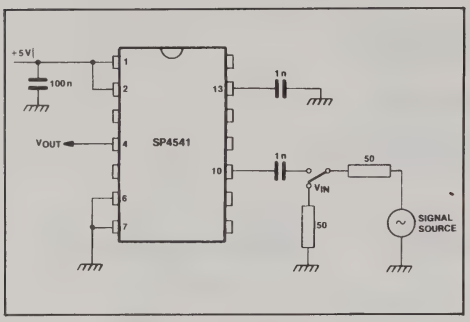

Fig.3 Test configuration

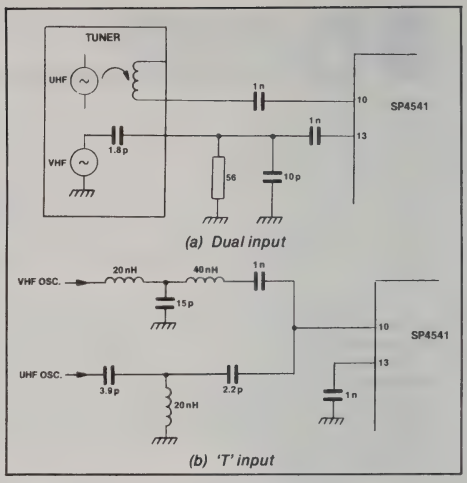

Fig.4 Combined input operation

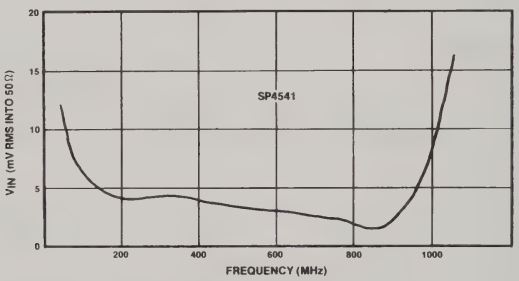

Fig.5 Typical input sensitivity

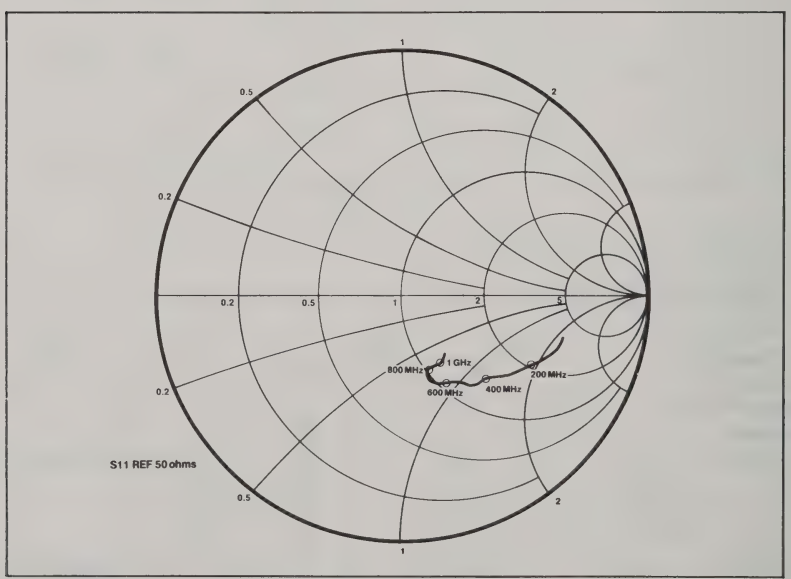

Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4632

1GHz ÷ 64 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4632 ÷ 64 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4632 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL outputs.

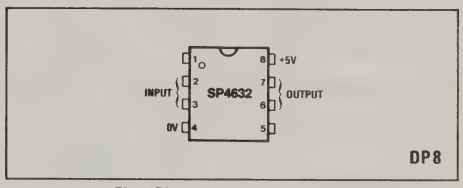

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C

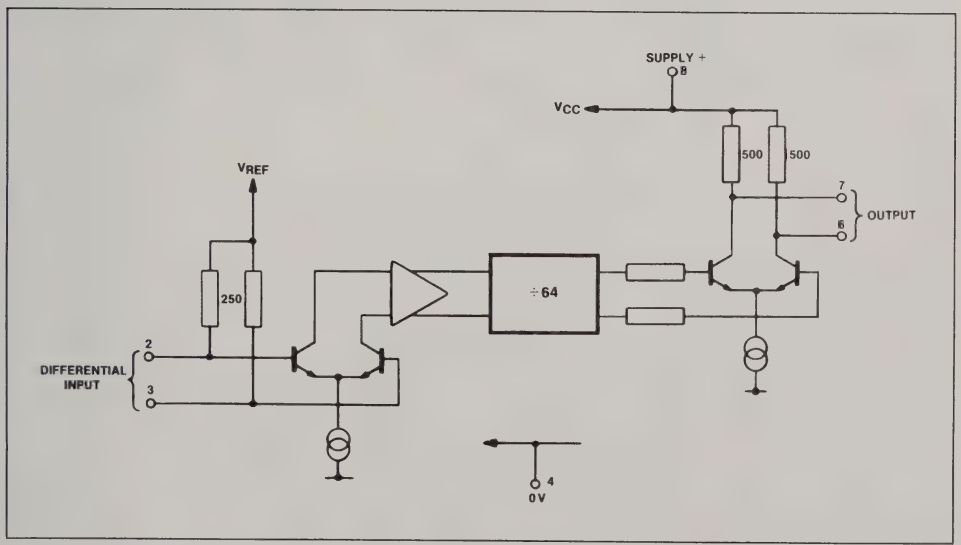

Fig.2 SP4632 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		25	35	mA	Vcc = 5V
Input sensitivity	2,3					RMS sinewave (50 ohms system)
80MHz			8	17.5	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1GHz			6	17.5	mV	
Input overload	2,3	200			mV	80MHz to 1GHz operating frequency
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz Vcc = 5V
	7	0.8			V p-p	fin = 1GHz Vcc = 5V
Output voltage with load as Fig.3	6	0.55			V	
	7	0.55			V	
Output impedance	6		0.5		kohms	
	7		0.5		kohms	
Output imbalance	6,7		0.1		V	

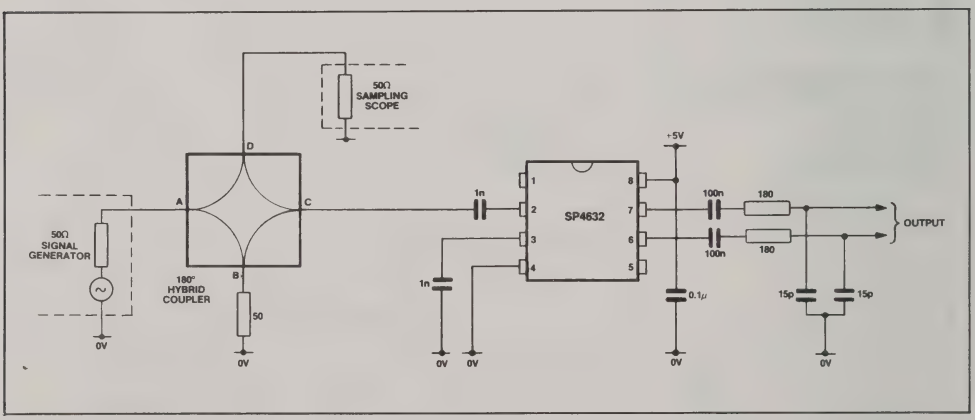

Fig.3 Test circuit

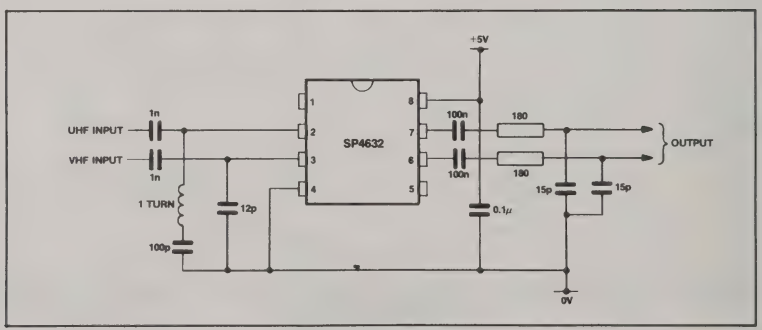

Fig.4 Application circuit

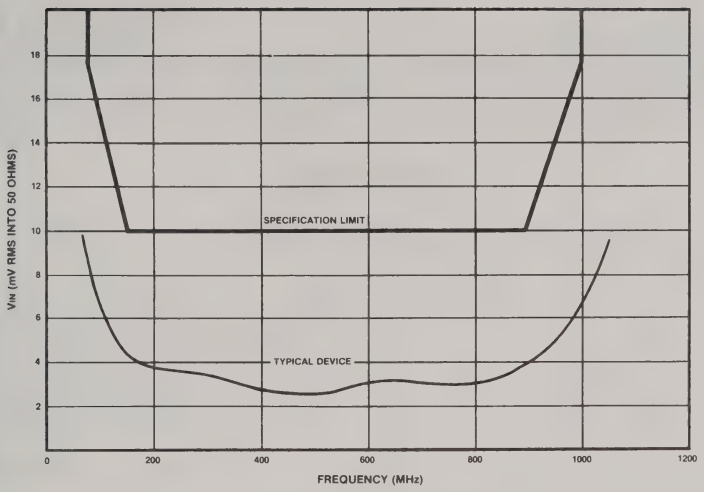

Fig.5 Typical input sensitivity

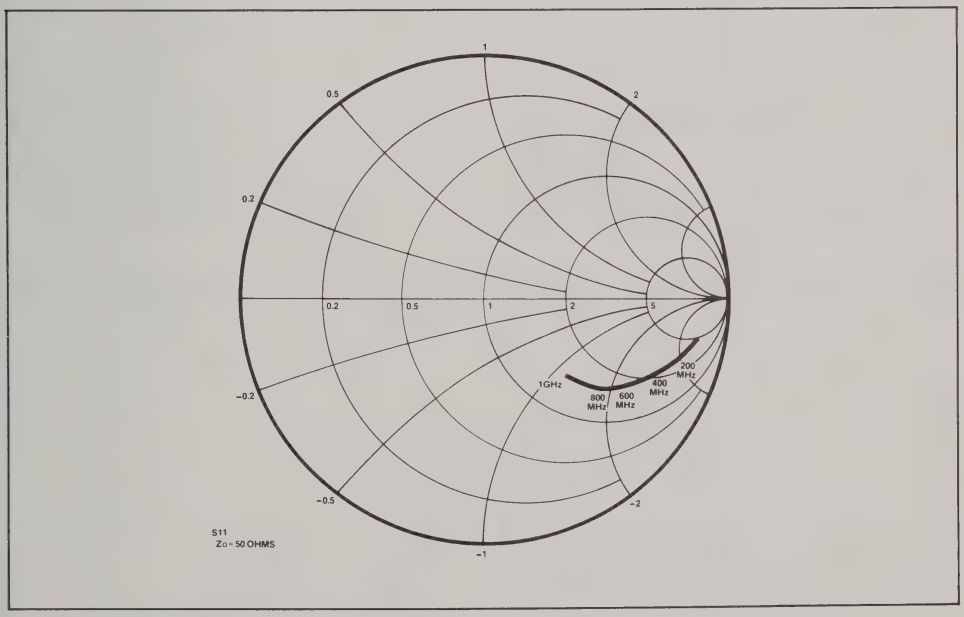

Fig.6 Typical input impedance

PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SP4633

1GHz ÷ 64 NON SELF OSCILLATING PRESCALER

The SP4633 ÷ 64 prescaler is one of Plessey Semiconductors latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4633 incorporates a two stage preamplifier which gives good low frequency sensitivity and prevents self oscillation.

Electrostatic protection is provided on all pins.

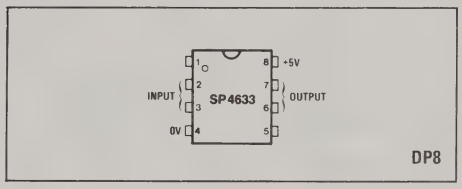

Fig.1 Pin connections - top view

FEATURES

- Does Not Self Oscillate
- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C

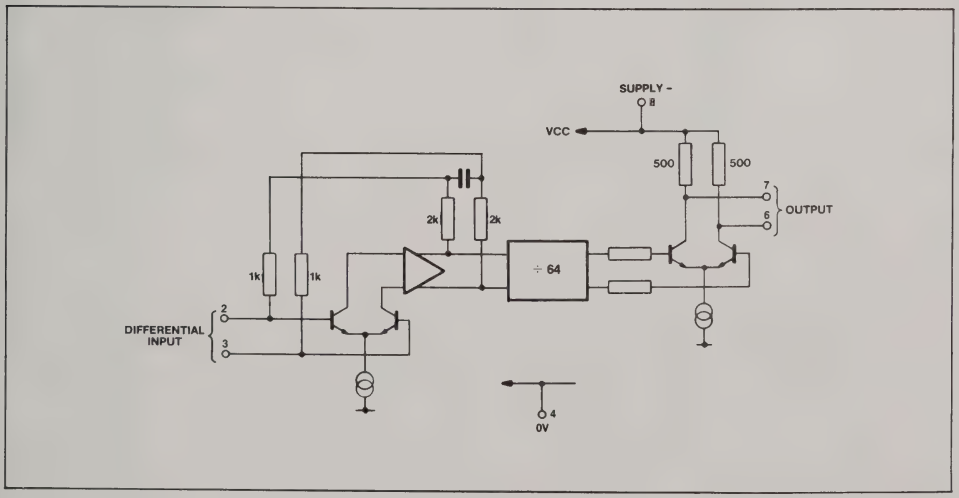

Fig.2 SP4633 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	V_{CC} + 5V
Input sensitivity	2,3					RMS sinewave (50 ohms system)
50MHz to 400MHz			1.5	5	mV	
600MHz			2	7.5	mV	
800MHz			3	10	mV	
1000MHz			5	15	mV	
Input overload	2,3	300			mV	50MHz to 1GHz operating frequency
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	0.8			V p-p	f_{in} = 1GHz V_{CC} = 5V
	7	0.8			V p-p	
Output voltage with load as Fig.3	6	0.55			V	f_{in} = 1GHz V_{CC} = 5V
	7	0.55			V	
Output impedance	6		0.5		kohms	
	7		0.5		kohms	
Output imbalance	6,7		0.1		V	

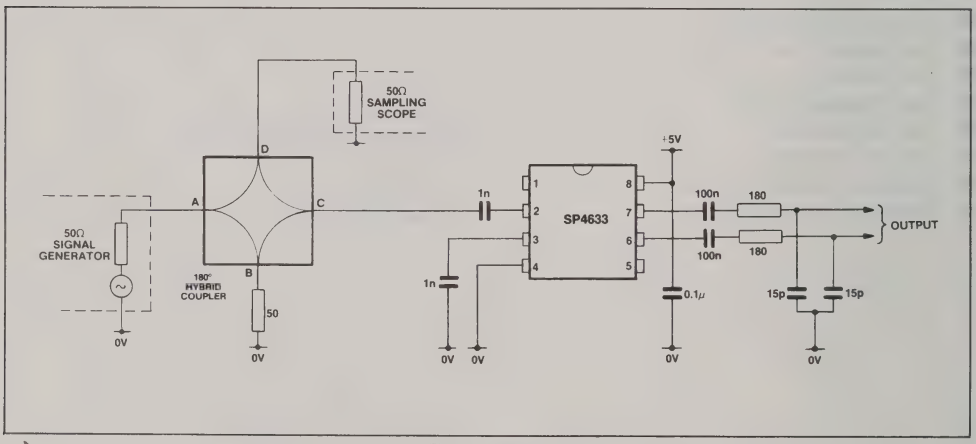

Fig.3 Test circuit

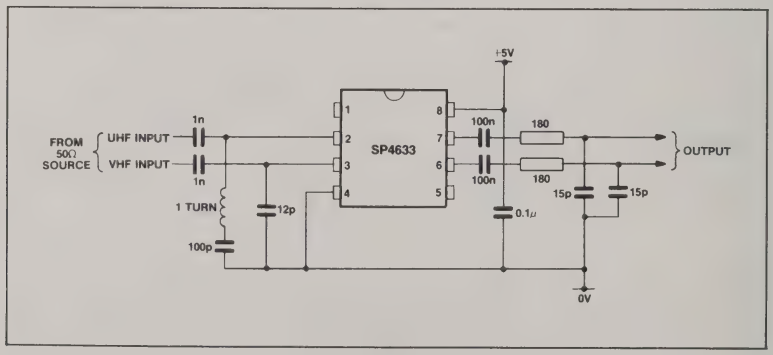

Fig.4 Application circuit

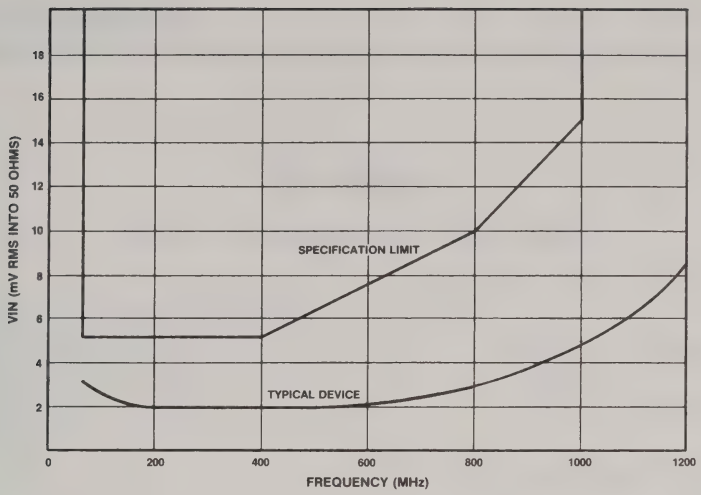

Fig.5 Typical input sensitivity

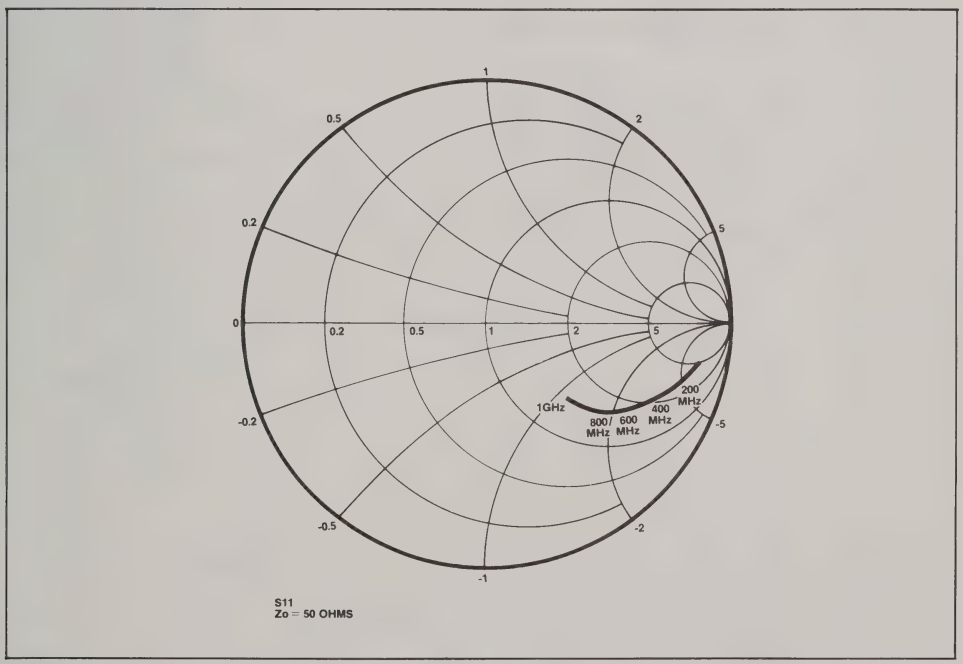

Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4634

1GHz ÷ 64 DUAL INPUT PRESCALER

The SP4634 is one of the new range of Plessey consumer high speed dividers which offer improved input sensitivity, higher input impedance and lower supply current. The device is intended for use in television frequency synthesis systems and has separate VHF, UHF inputs with a common reference. A band select input controls which of the prescaler input ports is active. It has a division ratio of 64 with complementary outputs.

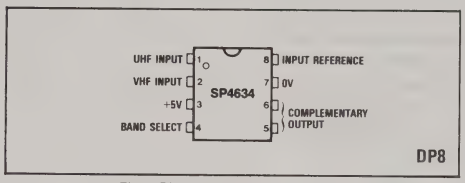

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current, Low Dissipation
- On Chip Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Low Output Radiation
- Complementary Output
- Dual Input Ports for VHF, UHF with Common Reference
- TTL, MOS Compatible Band Select Input

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7V max.
Supply current	200mA max.
Power dissipation	350mW max.
Band change voltage	18V max.
Input voltage	2.5V p-p max.
Storage temperature	-55° C to +125° C

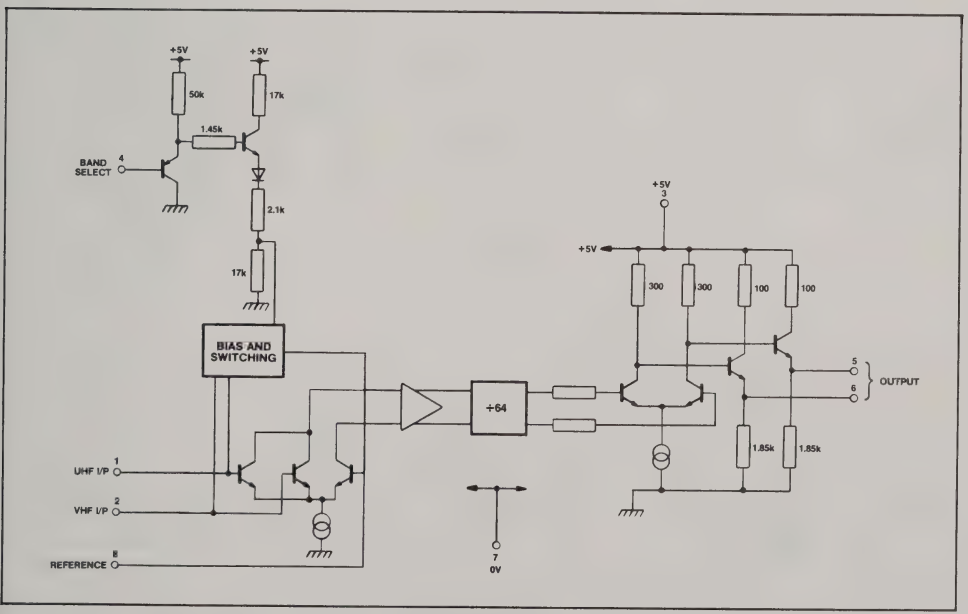

Fig.2 SP4634 diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} =0° C to +70° C; V_{CC} = +4.5V to +5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	3		30	45	mA	V_{CC} = 5V
Band change high level input voltage, V_{IH}	4	2		12	V	
Band change low level input voltage, V_{IL}	4	-0.5		0.8	V	
Band change high level input current	4			2	mA	V_{IH} = 12V DC
Band change low level input current	4			-1	mA	
Output voltage load as Fig.3	5,6	0.7	1.05		V p-p	F_{OUT} = 15MHz, V_{CC} = 5V,
Output voltage no load		0.9	1.20		V p-p	F_{OUT} = 15MHz V_{CC} = 5V
VHF sensitivity	2					V Pin 4 = 0.8V
Sinewave into 50Ω						
80 to 100MHz				14	mV rms	
100 to 500MHz				10	mV rms	
VHF overload		500			mV rms	80MHz to 1GHz operating frequency
UHF sensitivity	1					V Pin 4 = 2V
Sinewave into 50Ω						
80 to 100MHz				14	mV rms	
100 to 950MHz				10	mV rms	
950 to 1000MHz				17.5	mV rms	
UHF overload		500			mV rms	80MHz to 1GHz operating frequency
Output imbalance	5,6		0.1		V p-p	
Output impedance	5,6		20		Ohms	

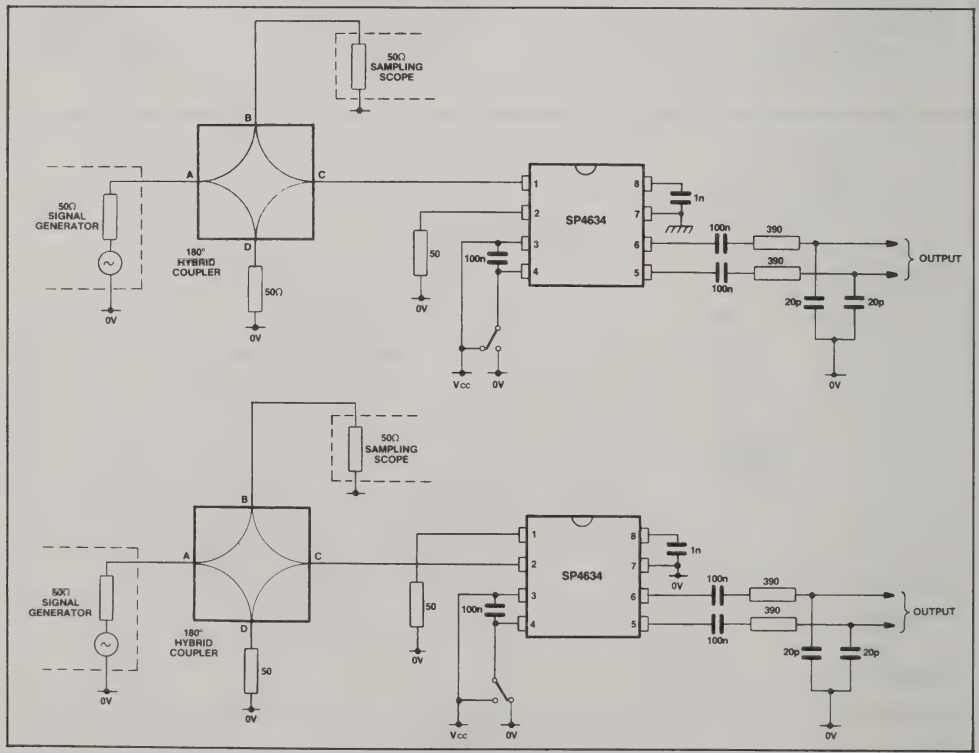

Fig.3 Test circuit

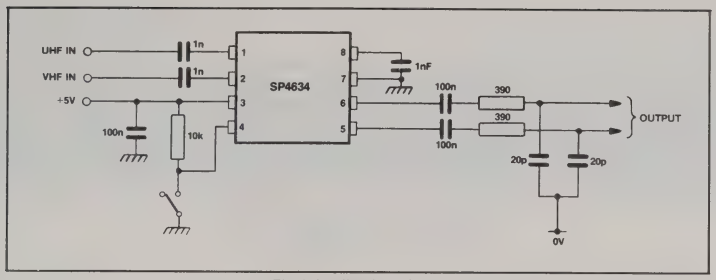

Fig.4 Application circuit

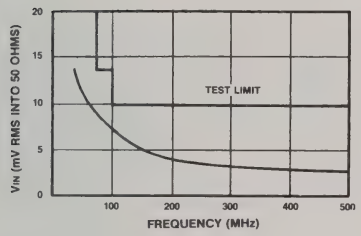

Fig.5 Typical VHF input sensitivity

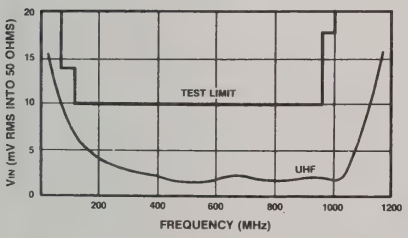

Fig.6 Typical UHF input sensitivity

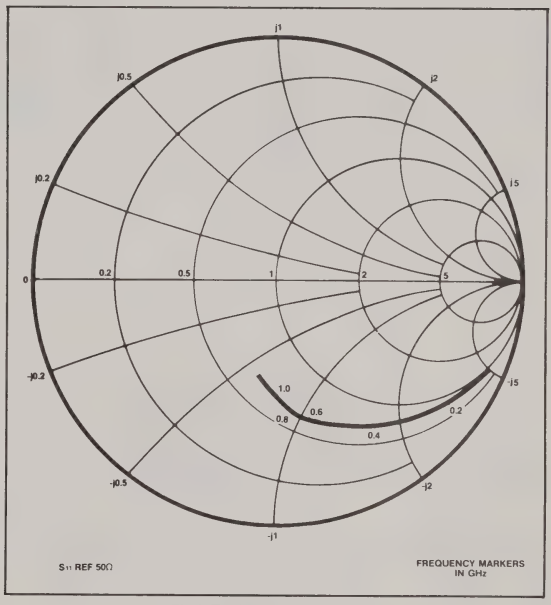

Fig.7 Typical input impedance

PLESSEY
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PRELIMINARY INFORMATION

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SP4636 EXP

1GHz ÷ 64 NON SELF OSCILLATING PRESCALER WITH HIGH OUTPUT SWING

The SP4636 ÷ 64 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. The device features a low supply current giving reduced dissipation and operating temperatures and is encapsulated in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4636 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL output.

Electrostatic protection is provided on all pins.

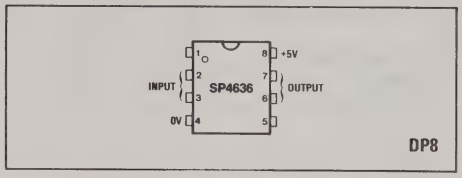

Fig.1 Pin connections - top view

FEATURES

- Does Not Self Oscillate
- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity From 50MHz to 1GHz
- High Input Impedance
- Balanced ECL Outputs
- High Output Swing
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C

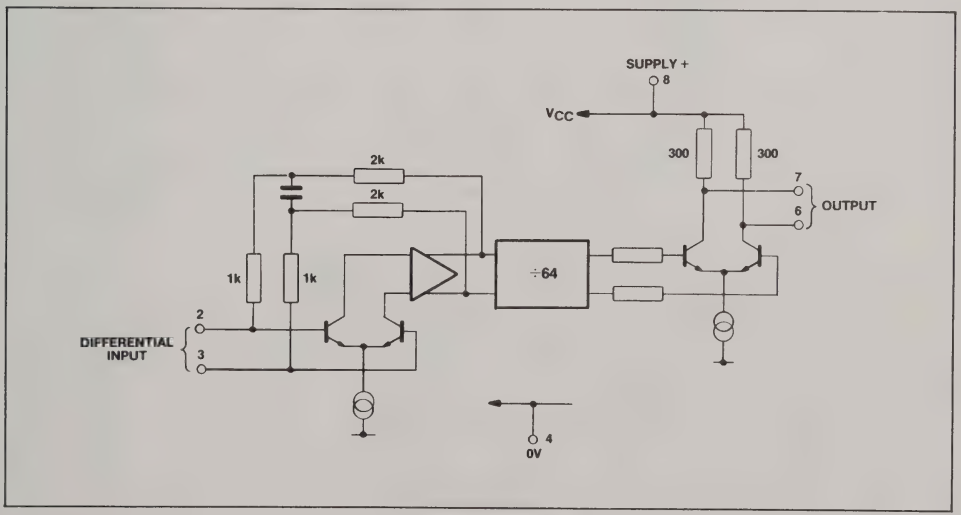

Fig.2 SP4636 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave (50 ohms systems)
50MHz to 400MHz			1.5	5	mV	
600MHz			2	7.5	mV	
800MHz			3	10	mV	
1000MHz			5	15	mV	
Input overload	2,3	300			mV	50MHz to 1GHz
					mV	operating frequency
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	1.0			V p-p	fin = 1GHz V_{CC} = 5V
	7	1.0			V p-p	
Output voltage load	6	tbd			V p-p	fin = 1GHz V_{CC} = 5V
as Fig.3	7	tbd			V p-p	
Output impedance	6		0.3		kohms	
	7		0.3		kohms	
Output imbalance	6,7			0.1	V	

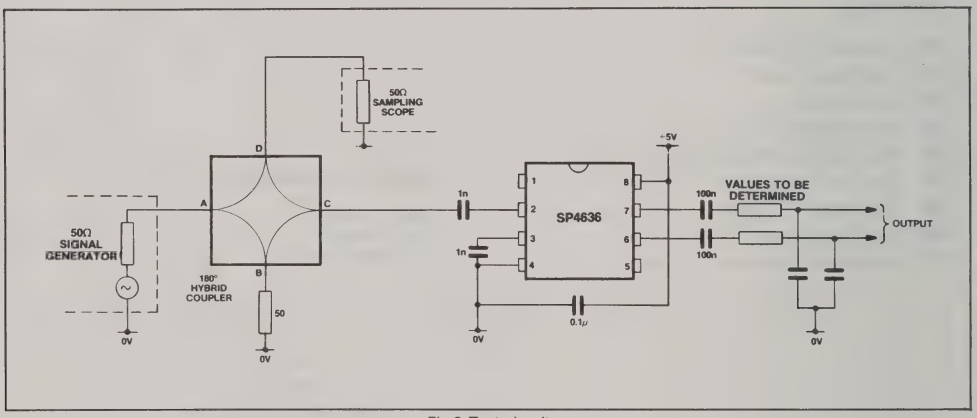

Fig.3 Test circuit

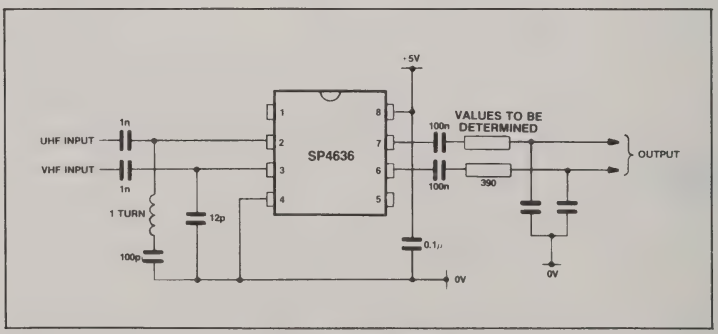

Fig.4 Application circuit

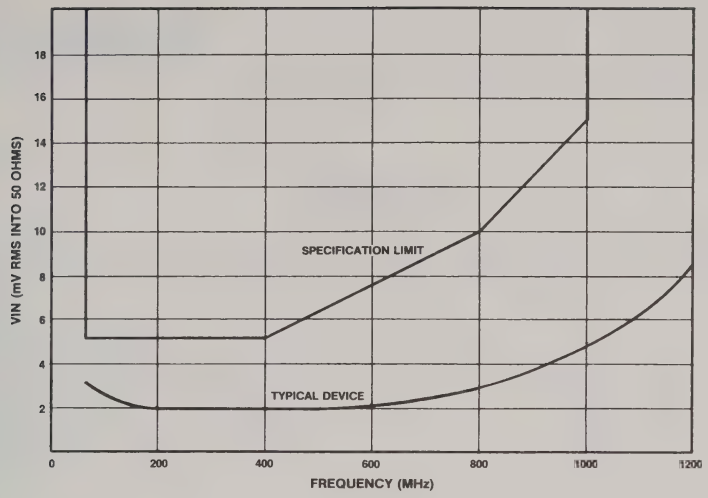

Fig.5 Typical input sensitivity

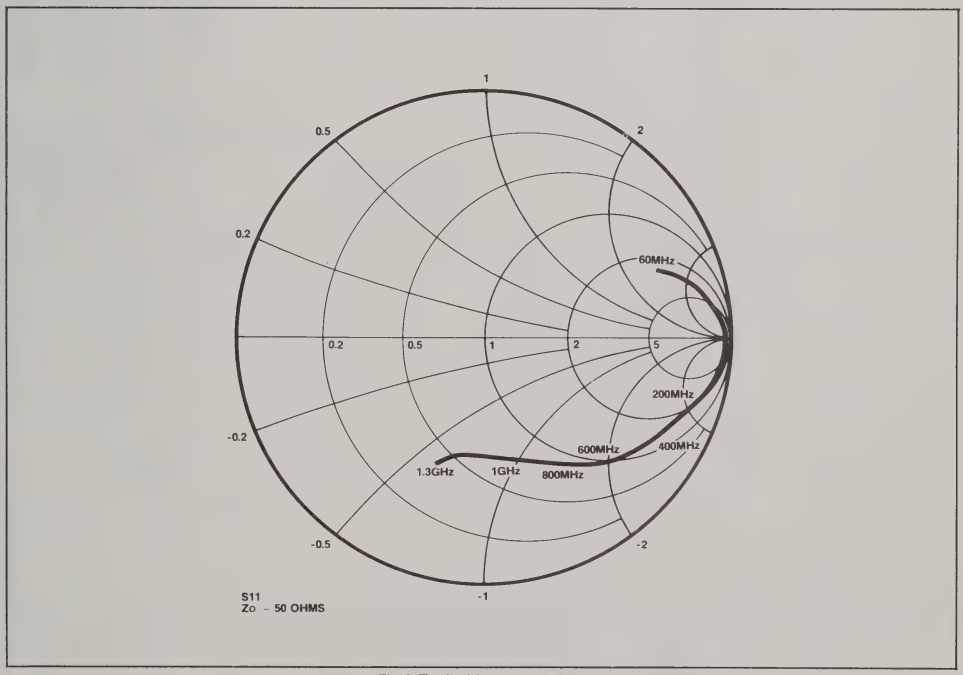

Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4642

1GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4642 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4642 incorporates an on-chip preamplifier with differential inputs, and has a single TTL output.

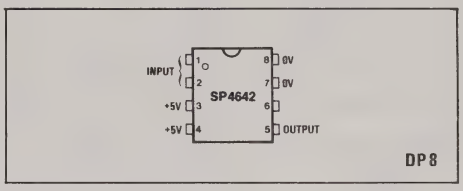

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- TTL Output

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C

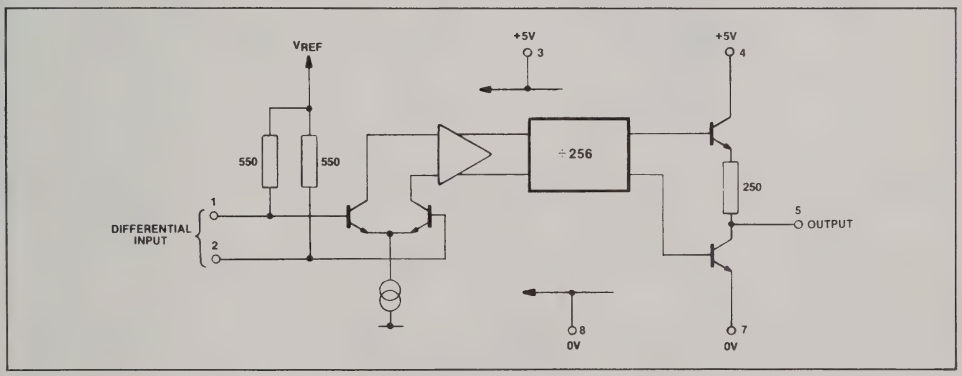

Fig.2 SP4642 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	3,4		25	35	mA	V_{CC} = 5V
Input sensitivity	1,2					RMS sinewave
80MHz			8	17.5	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1GHz			6	17.5	mV	
Input overload	1,2	200			mV	80MHz to 1GHz operating frequency
Input impedance	1,2		50		ohms	See Fig.6
			2		pF	
Output voltage						
High	5	3.3			V	Sourcing 0.2mA V_{CC} = 5V, fin = 1GHz
Low	5			0.4	V	Sinking 2mA V_{CC} = 5V, fin = 1GHz

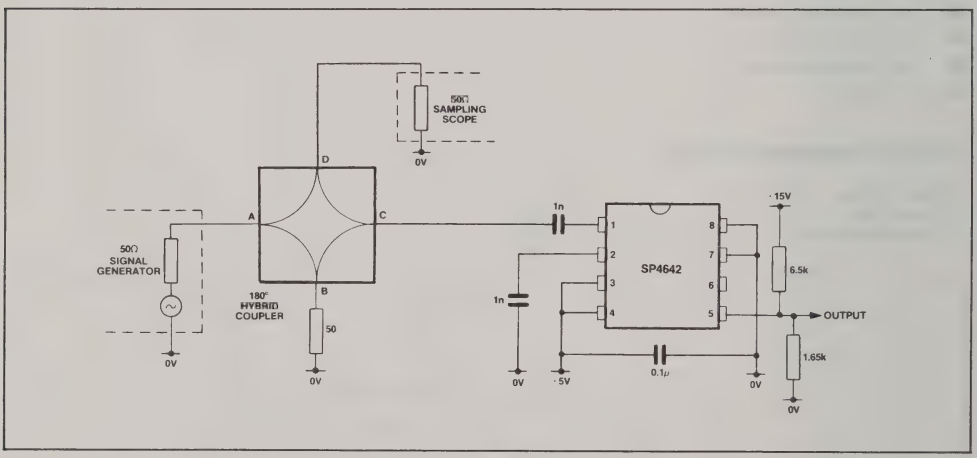

Fig.3 Test circuit

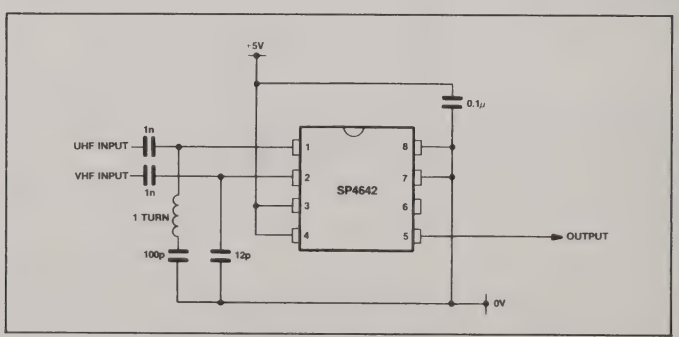

Fig.4 Application circuit

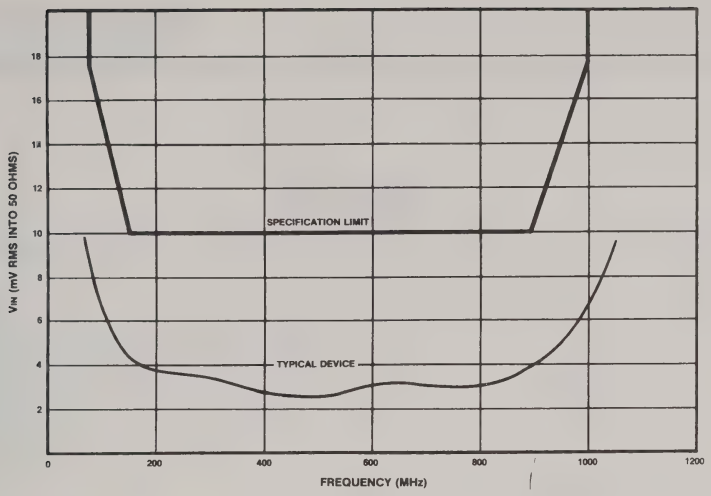

Fig.5 Typical input sensitivity

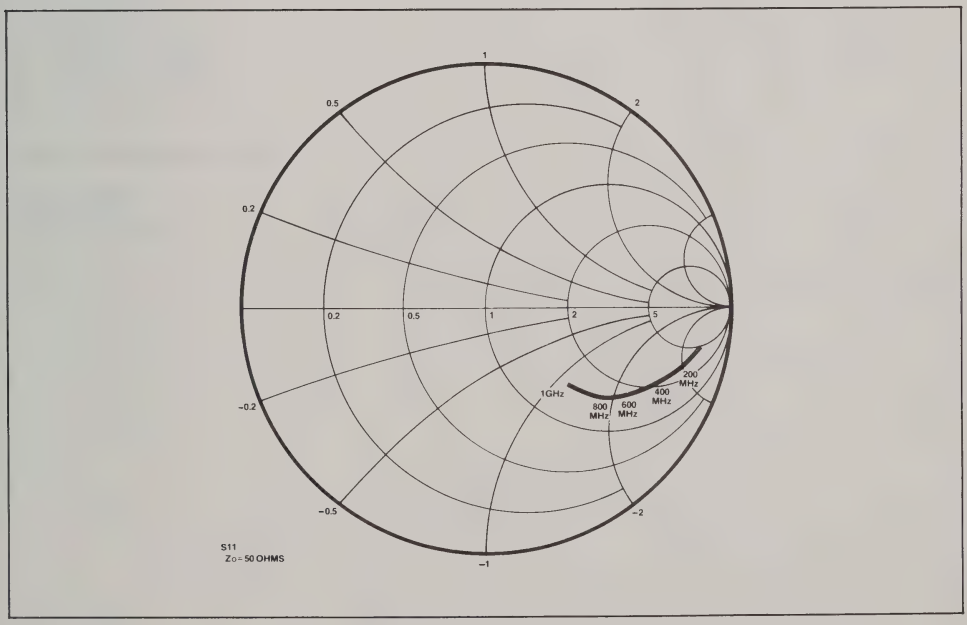

Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4652

1GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4652 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4652 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL outputs.

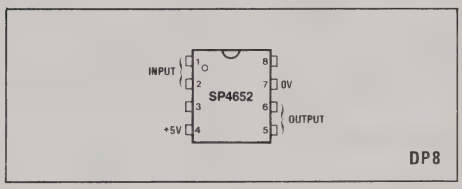

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C

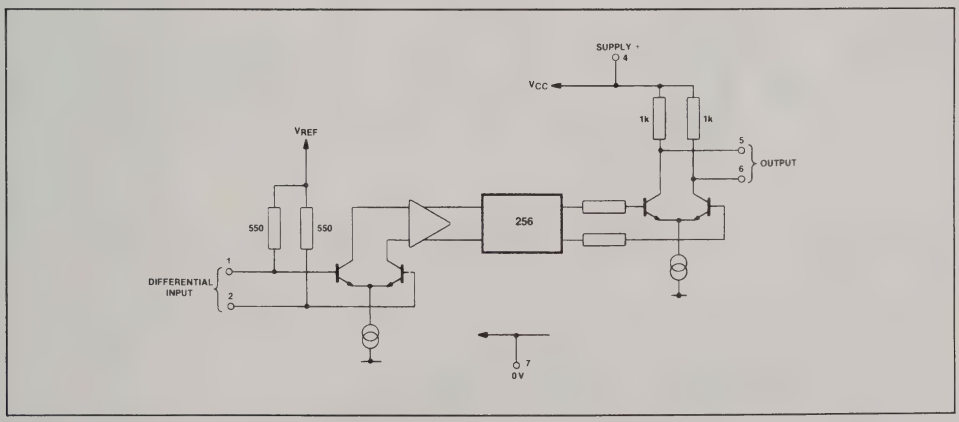

Fig.2 SP4652 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	4		25	35	mA	V_{CC} = 5V
Input sensitivity	1,2					RMS sinewave
80MHz			8	17.5	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1GHz			6	17.5	mV	
Input overload	1,2	200			mV	80MHz to 1GHz operating frequency
Input impedance	1,2		50		ohms	See Fig.6
			2		pF	
Output voltage no load	5	0.8			V p-p	fin = 1GHz V_{CC} = 5V
	6	0.8			V p-p	
Output voltage load as Fig.3	5	0.6			V	fin = 1GHz V_{CC} = 5V
	6	0.6			V	
Output impedance	5		1		kohms	
	6		1		kohms	
Output imbalance	5,6		0.1		V	

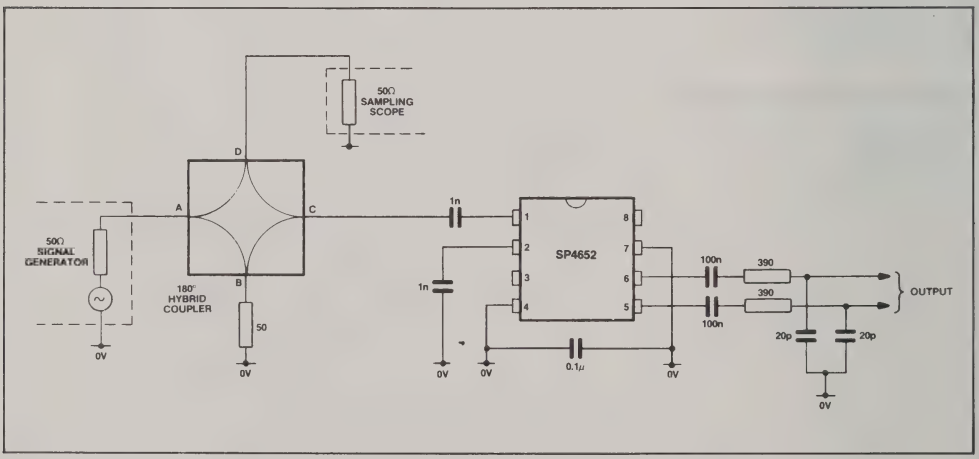

Fig.3 Test circuit

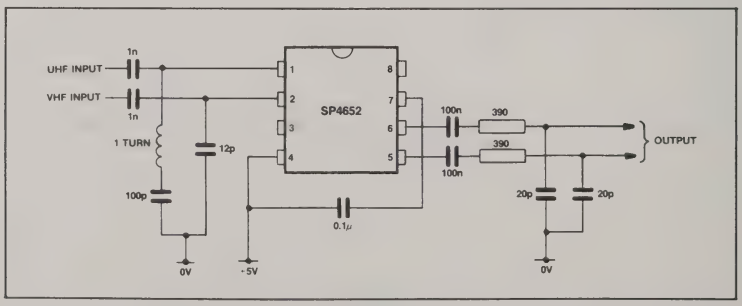

Fig.4 Application circuit

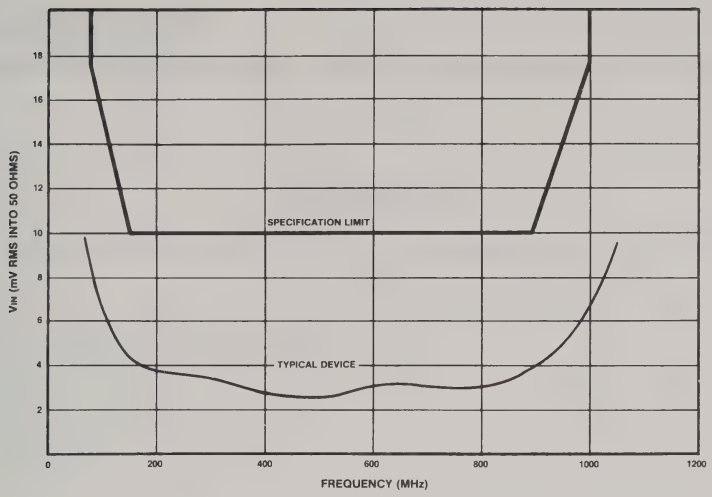

Fig.5 Typical input sensitivity

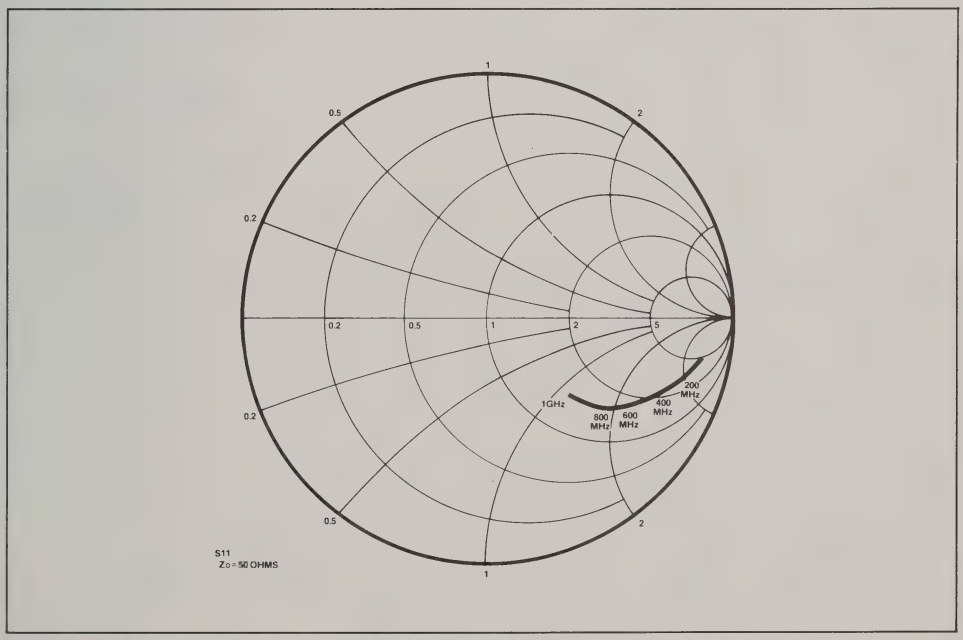

Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP4653

1GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4653 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4653 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL outputs.

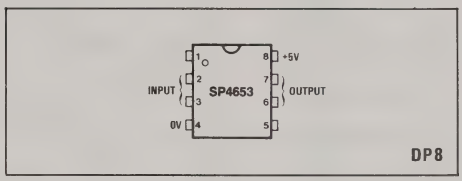

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C

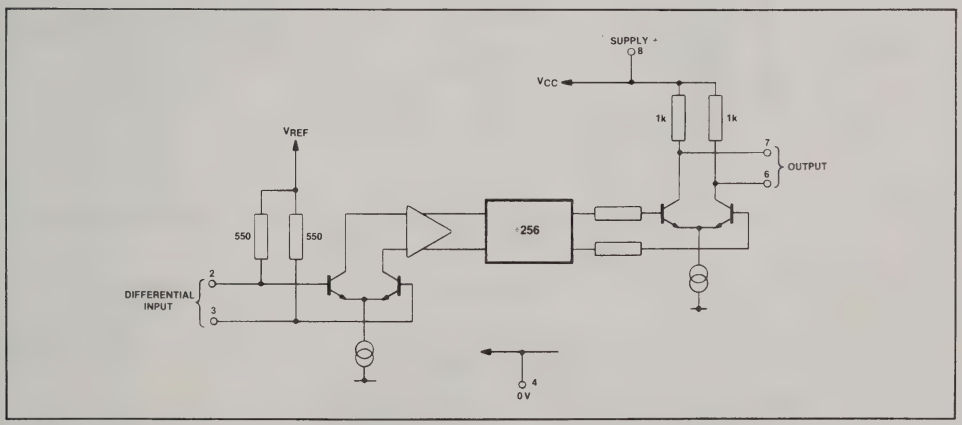

Fig.2 SP4653 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		25	35	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
70MHz			8	14	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1050MHz			6	14	mV	
Input overload	2,3	200			mV	70MHz to 1050MHz operating frequency
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz V_{CC} = 5V
	7	0.8			V p-p	
Output voltage load as Fig.3	6	0.6			V p-p	fin = 1GHz V_{CC} = 5V
	7	0.6			V p-p	
Output impedance	6		1		kohms	
	7		1		kohms	
Output imbalance	6,7		0.1		V	

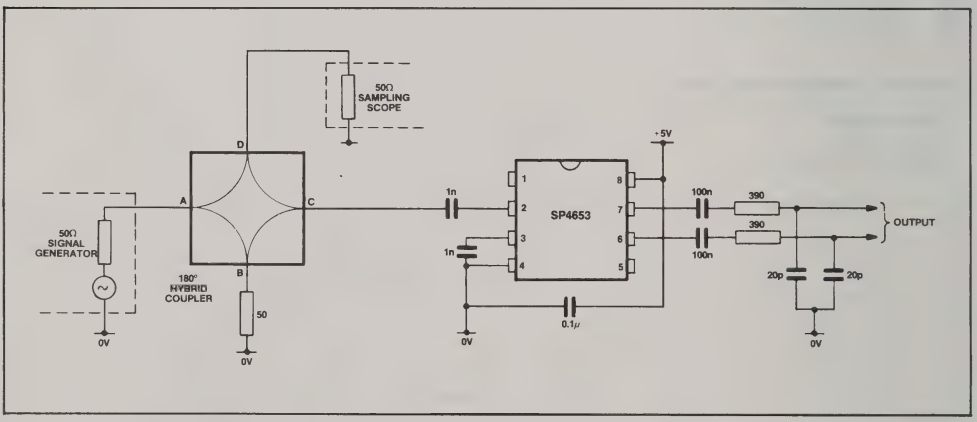

Fig.3 Test circuit

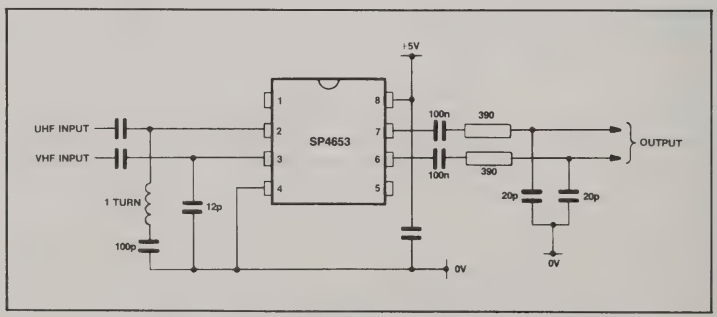

Fig.4 Application circuit

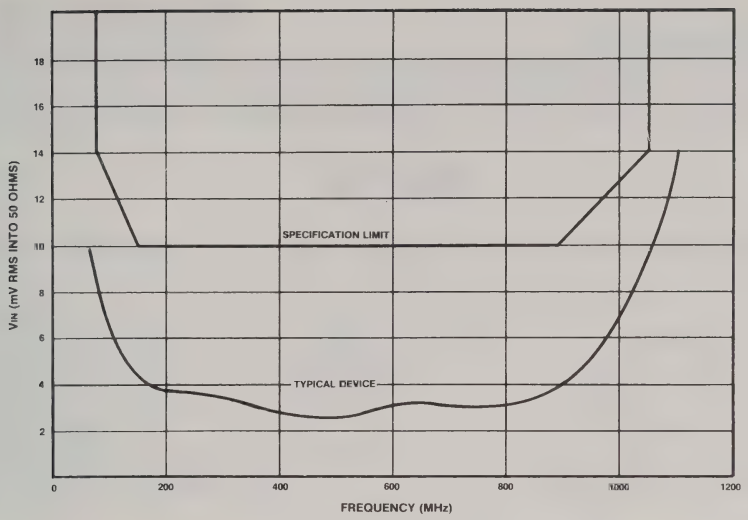

Fig.5 Typical input sensitivity

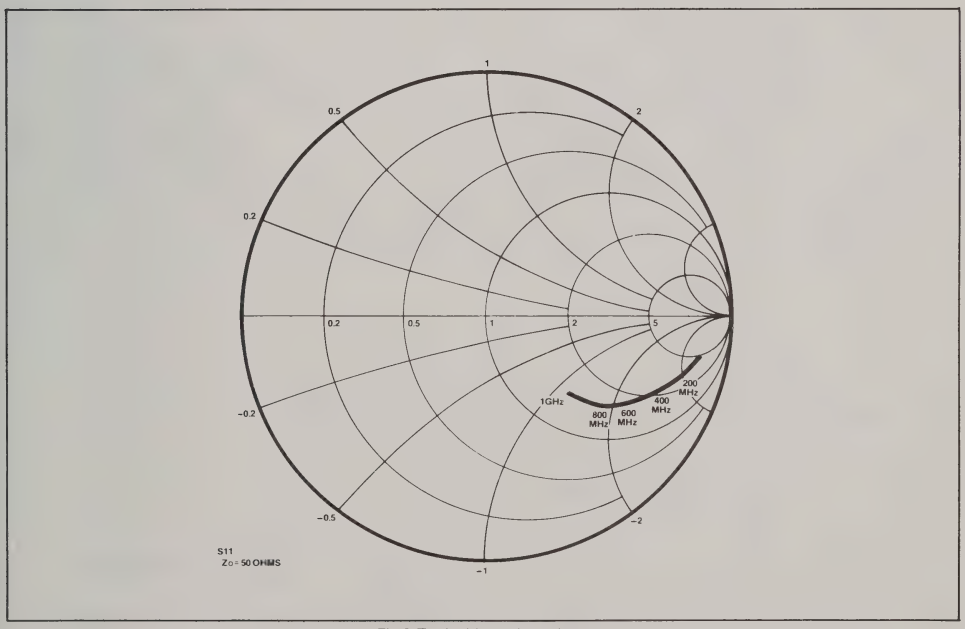

Fig.6 Typical input impedance

PLESSEY
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Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SP4660

1GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4660 ÷ 256 prescaler is one of Plessey Semiconductors' lastest range of high speed dividers for consumer frequency synthesis and measurement systems. The device features a low supply current giving reduced dissipation and operating temperatures and is encapsulated in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4660 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL output.

Electrostatic protection is provided on all pins.

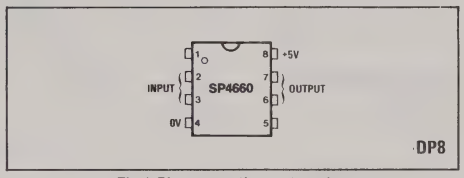

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity from 50MHz to 1GHz
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C

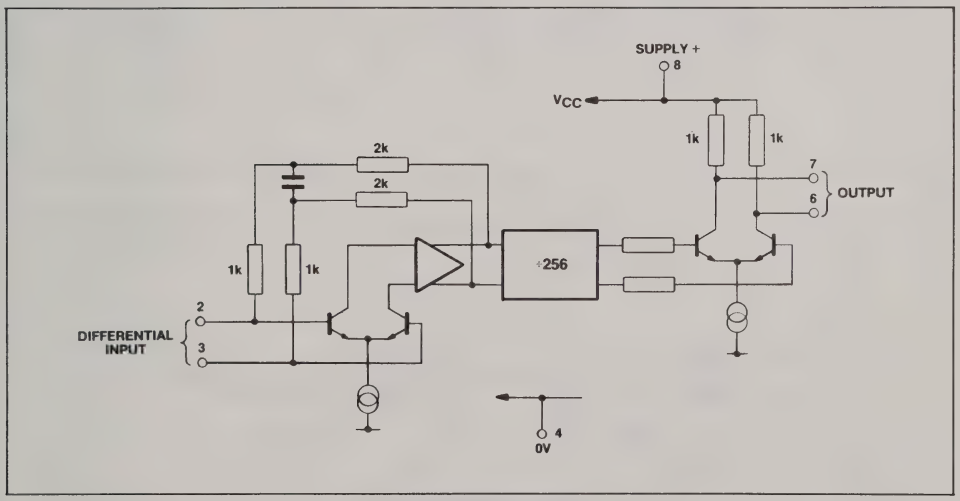

Fig.2 SP4660 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz V_{CC} = 5V
	7	0.8			V p-p	fin = 1GHz V_{CC} = 5V
Output voltage load	6	0.6			V p-p	
as Fig.3	7	0.6			V p-p	
Output impedance	6		1		kohms	
	7		1		kohms	
Output imbalance	6,7			0.1	V	

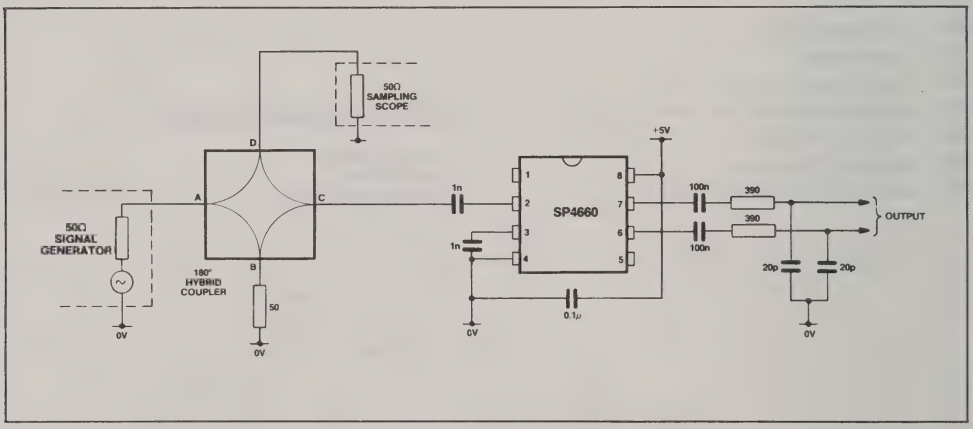

Fig.3 Test circuit

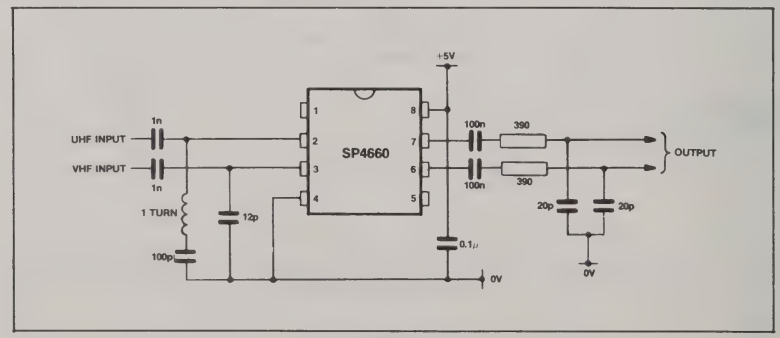

Fig.4 Application circuit

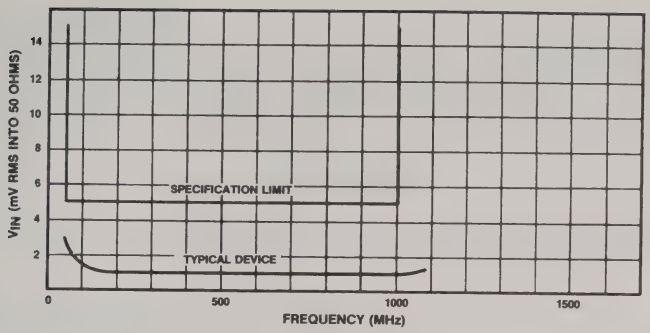

Fig.5 Typical input sensitivity

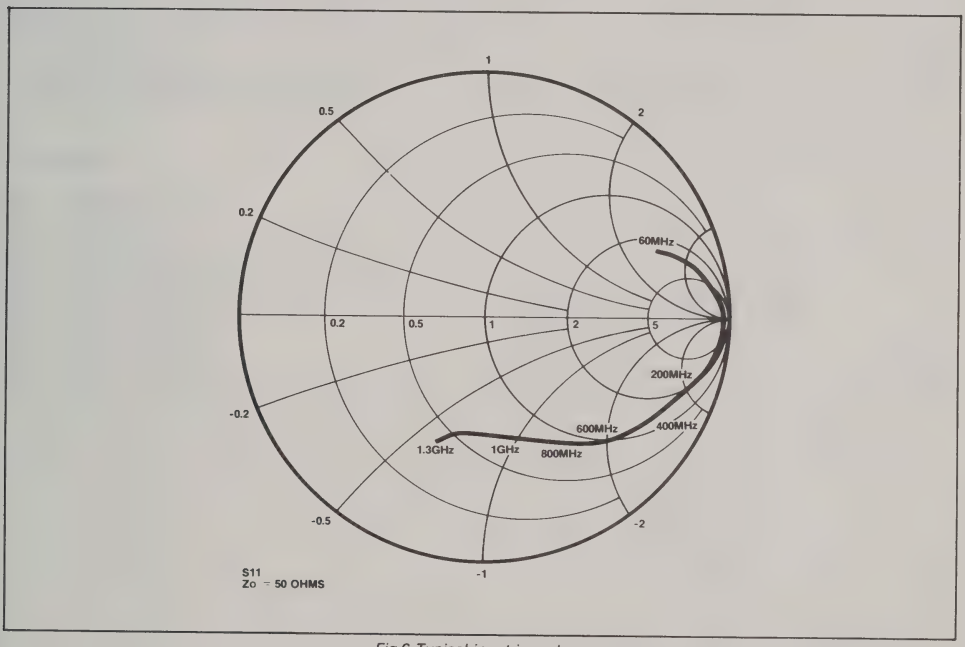

Fig.6 Typical input impedance

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SP4661

1GHz ÷ 256 NON SELF OSCILLATING PRESCALER

The SP4661 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. The device features a low supply current giving reduced dissipation and operating temperatures and is encapsulated in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4661 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL output.

Electrostatic protection is provided on all pins.

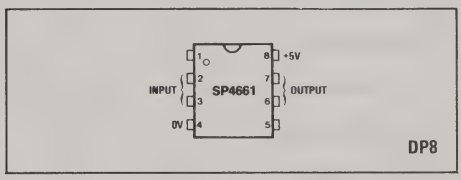

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity From 50MHz to 1GHz
- High Input Impedance
- Balanced ECL Outputs
- Non Self Oscillating
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C

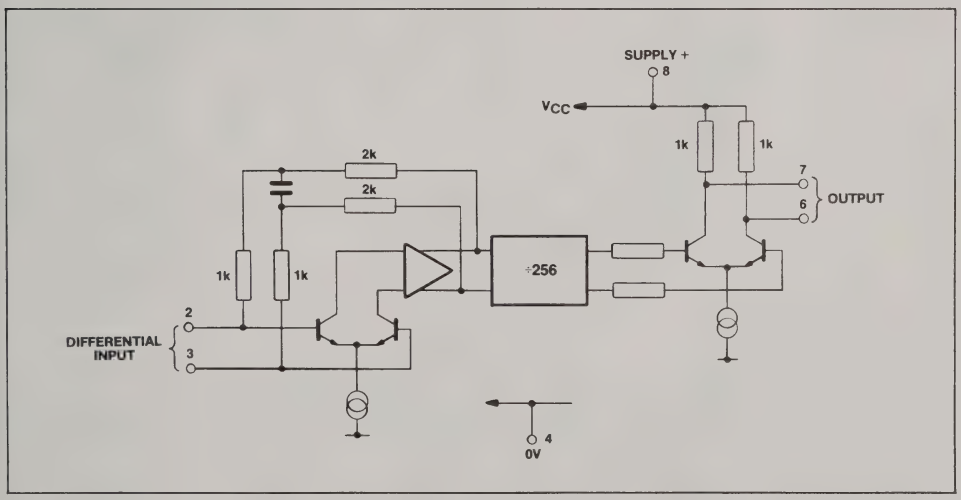

Fig.2 SP4661 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
50MHz to 400MHz			1.5	5	mV	
600MHz			2	7.5	mV	
800MHz			3	10	mV	
1000MHz			5	15	mV	
Input overload	2,3	300			mV	50MHz to 1000MHz
					mV	operating frequency
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz V_{CC} = 5V
	7	0.8			V p-p	
Output voltage load	6	0.6			V p-p	fin = 1GHz V_{CC} = 5V
as Fig.3	7	0.6			V p-p	
Output impedance	6		1		kohms	
	7		1		kohms	
Output imbalance	6,7			0.1	V	

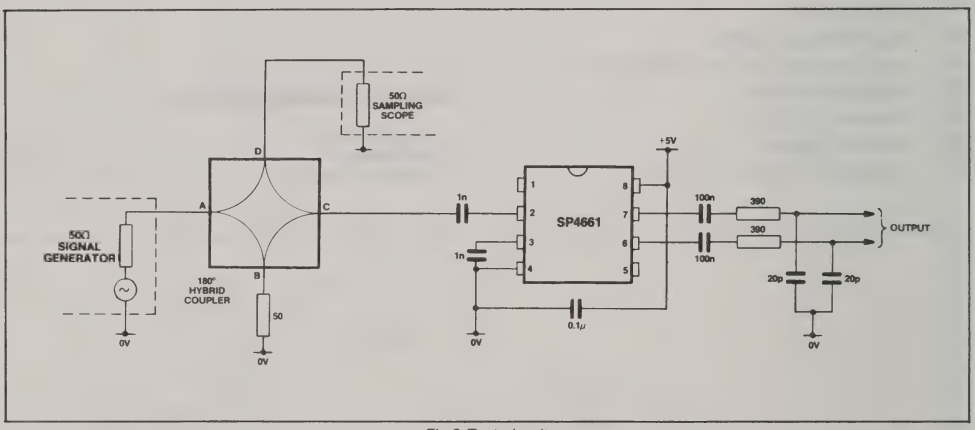

Fig.3 Test circuit

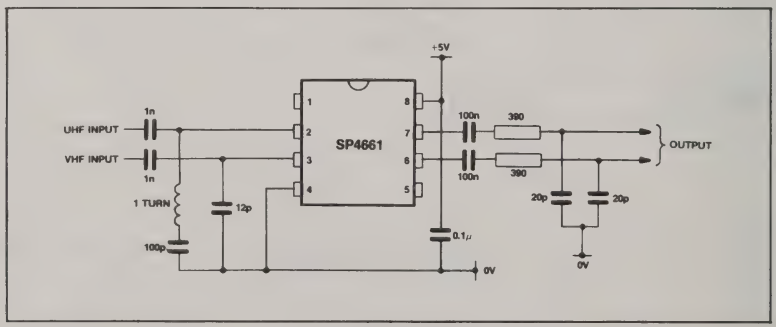

Fig.4 Application circuit

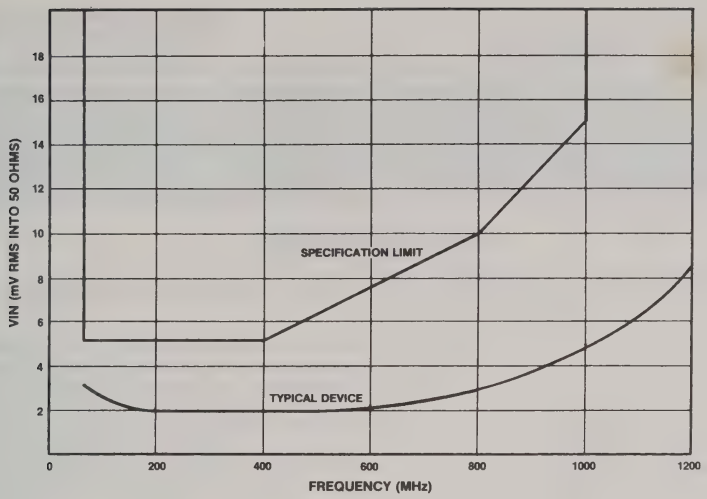

Fig.5 Typical input sensitivity

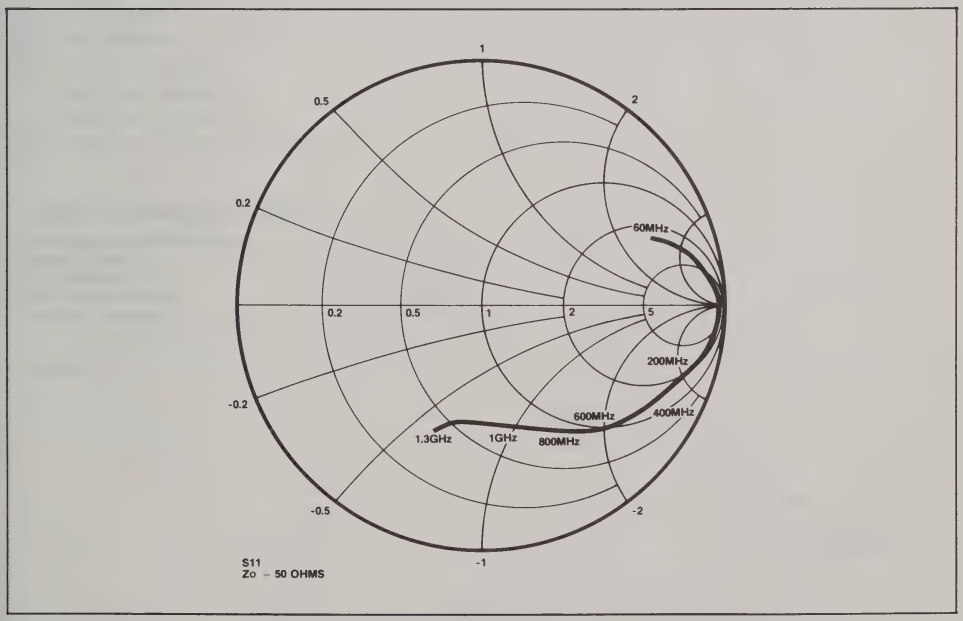

Fig.6 Typical input impedance

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SP4665 EXP

1GHz ÷ 64/256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4665 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4665 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL outputs.

Electrostatic protection is provided on all pins.

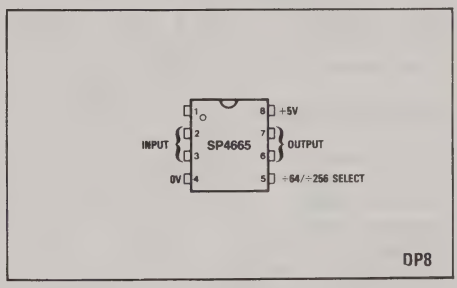

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-1° C to +80° C**
Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C
Junction temperature	+175° C

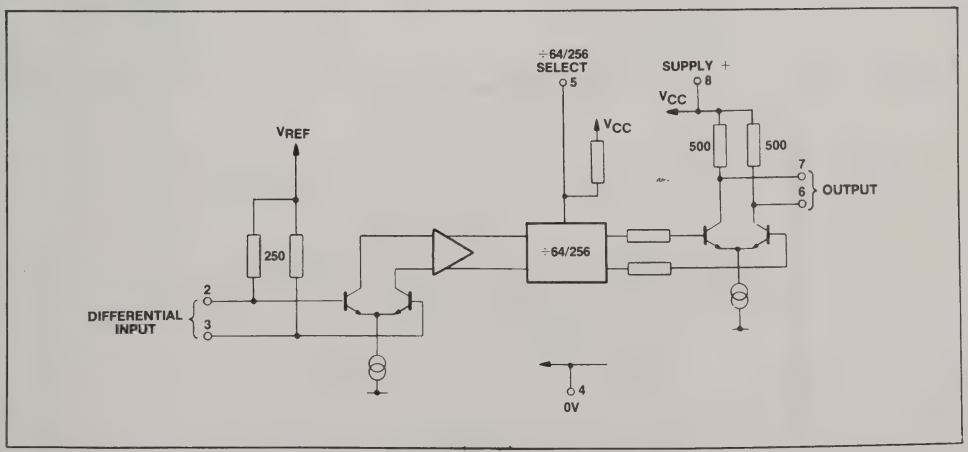

Fig.2 SP4665 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0° C to +80° C, V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		32	42	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
70MHz			8	22	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1050MHz			6	20	mV	
Input overload	2,3	300			mV	70MHz to 1050MHz operating frequency
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1GHz V_{CC} = 5V
	7	0.8			V p-p	
Output impedance	6		500		ohms	
	7		500		ohms	
Output imbalance	6,7		0.1		V	
Voltage for ÷256 operation	5			1	V	
Voltage for ÷64 operation	5	3.5			V	See Note 1
Sink current for ÷256 operation	5			100	μA	V Pin 5 = 0.3V_{CC}

NOTE 1. Pin 5 has an internal pull up and may be left open circuit for ÷64 operation.

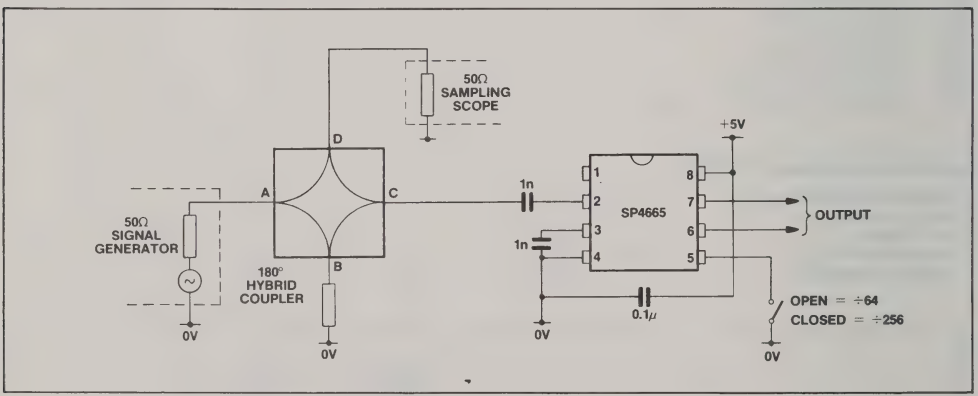

Fig.3 Test circuit

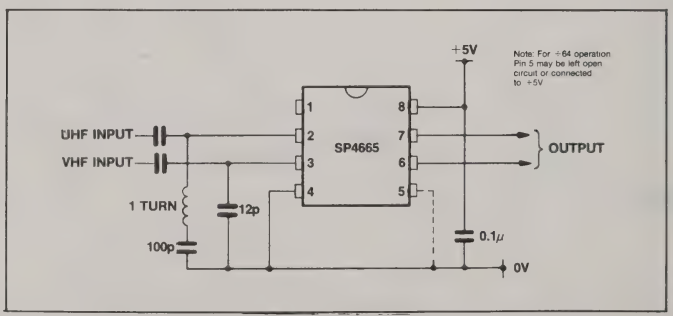

Fig.4 Application circuit

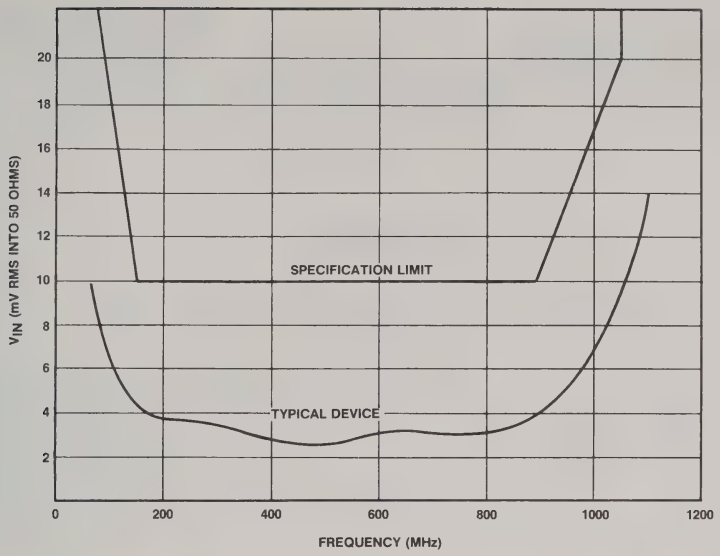

Fig.5 Typical input sensitivity

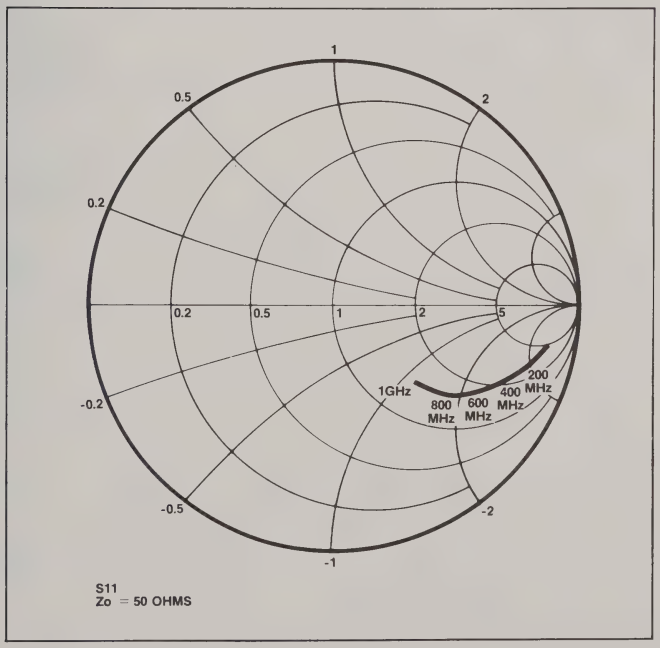

Fig.6 Typical input impedance

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SP4670

1GHz ÷ 380/400 DUAL MODULUS PRESCALER

The SP4670 ÷ 380/400 prescaler is one of Plessey Semiconductors latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8 pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4670 incorporates an on chip preamplifier with differential inputs and has a single ECL output. The control input is latched and synchronised making the device highly tolerant to delays in the control loop.

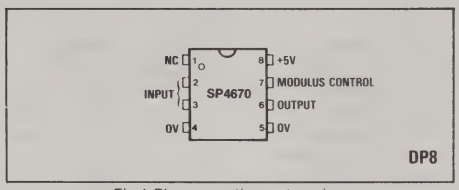

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- Latched and Synchronised Modulus Control Input
- Single ECL Output

ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vcc +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C
Control input voltage	-0.5V to Vcc

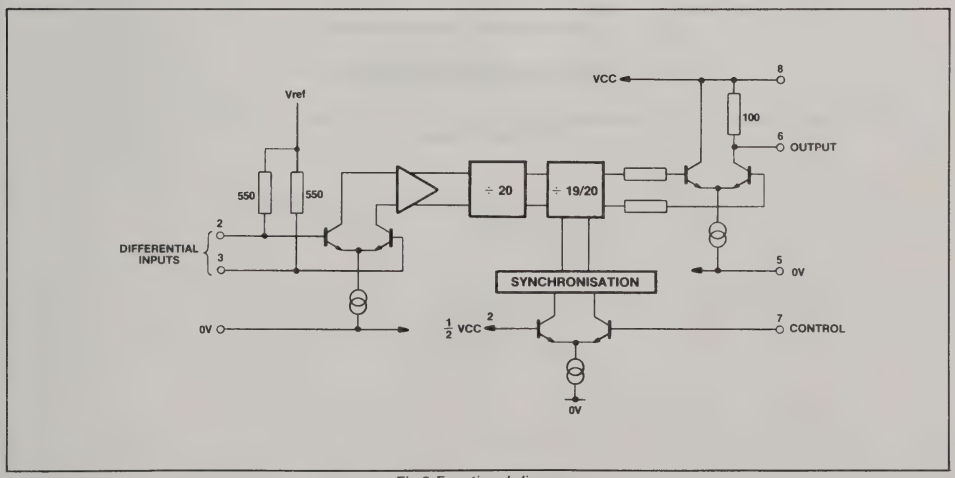

Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range	8	4.5		5.5	V	
Supply current	8		60	75	mA	
Input sensitivity	2,3					RMS sinewave (50 ohm system)
80MHz			8	17.5	mV	
150MHz			4	10	mV	
300MHz			3	10	mV	
500MHz			3	10	mV	
700MHz			3	10	mV	
900MHz			4	10	mV	
1GHz			6	17.5	mV	
Input overload						
80 to 450MHz	2,3	350			mV	
450MHz to 1GHz	2,3	200			mV	
Input impedance	2,3					See Smith chart
Output voltage	6	240	300	360	mV	Peak to peak, no load
Output impedance	6		100		ohms	
Control input current	7		10		μA	
Control input high voltage	7	2/3V_{CC}				
Control input low voltage	7			1/3V_{CC}		
Control input pulse width	7	200			ns	

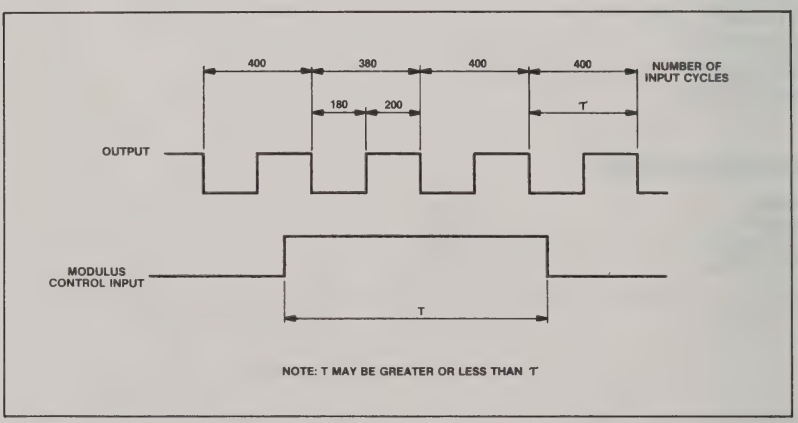

Fig.3 Timing diagram

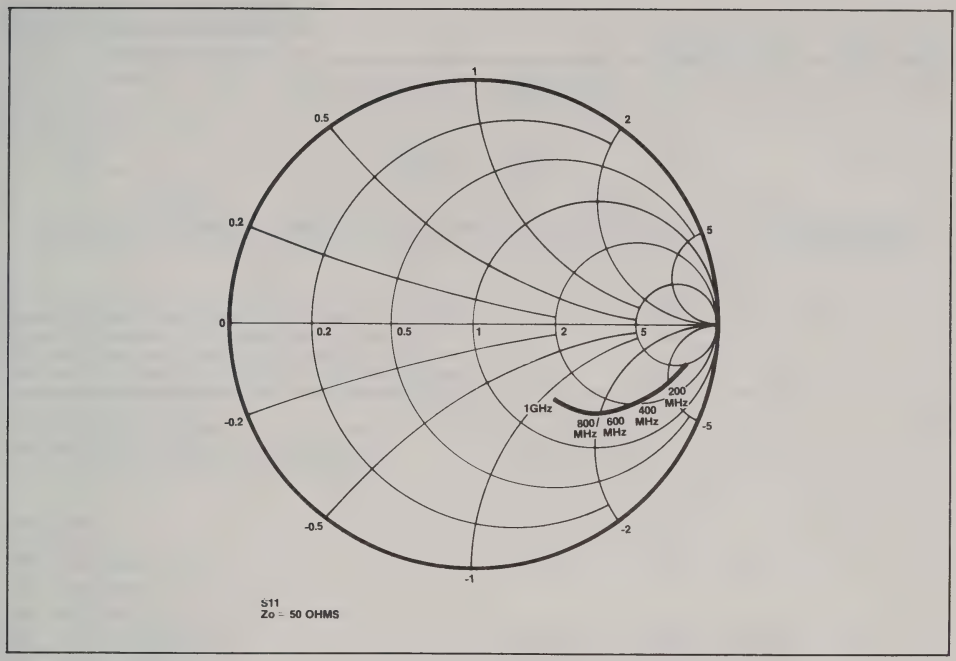

Fig.4 Typical input impedance

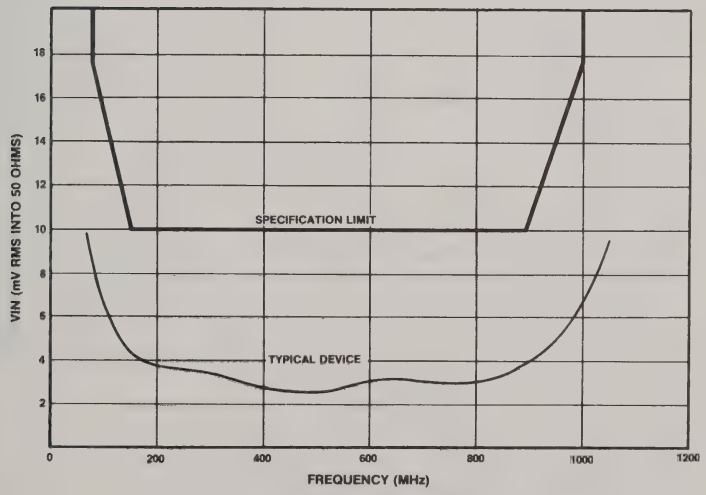

Fig.5 Typical input sensitivity

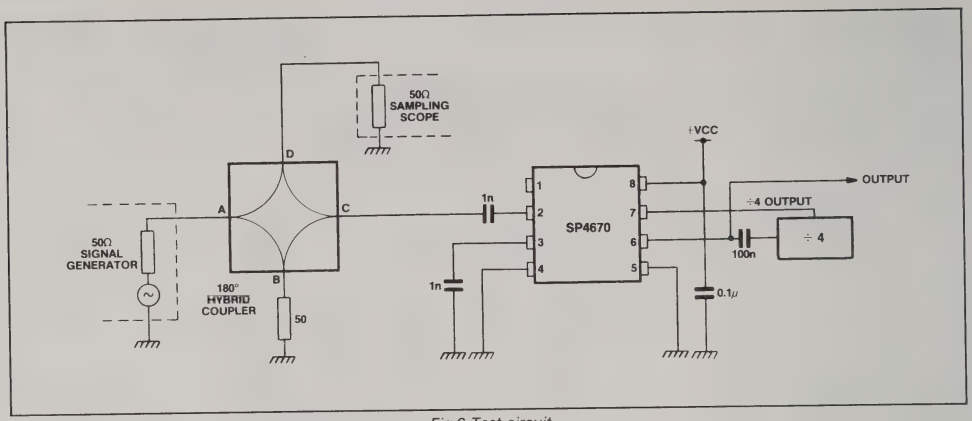

Fig.6 Test circuit

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SP4730

1.3GHz ÷ 64 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4730 ÷ 64 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. The device features a low supply current giving reduced dissipation and operating temperatures and is encapsulated in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4730 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL output.

Electrostatic protection is provided on all pins.

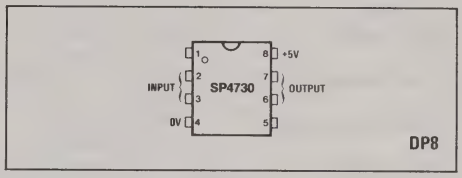

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C

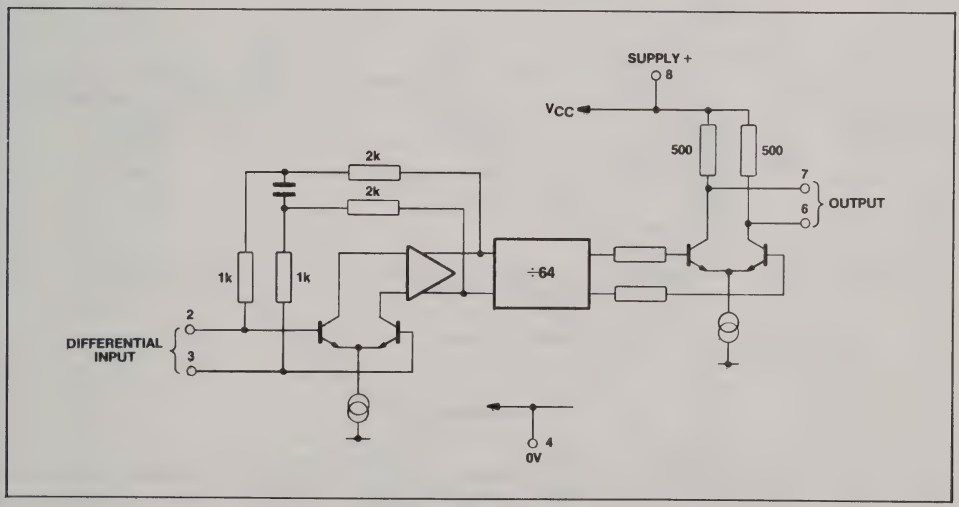

Fig.2 SP4730 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave (50 ohms system)
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1.3GHz V_{CC} = 5V
	7	0.8			V p-p	
Output voltage load	6	0.55			V p-p	fin = 1.3GHz V_{CC} = 5V
as Fig.3	7	0.55			V p-p	
Output impedance	6		0.5		kohms	
	7		0.5		kohms	
Output imbalance	6,7			0.1	V	

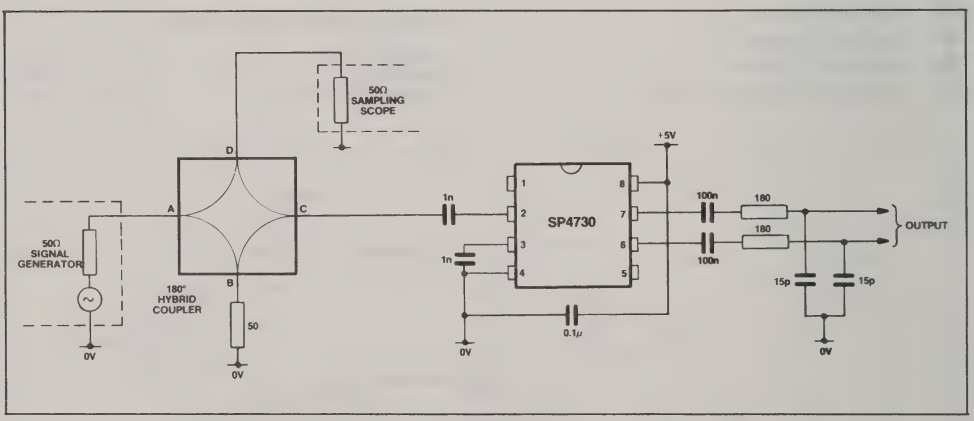

Fig.3 Test circuit

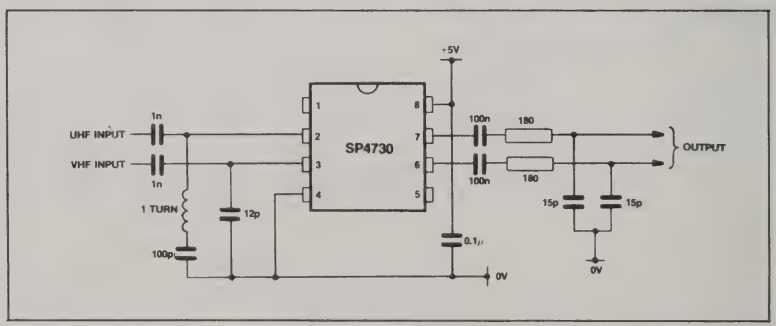

Fig.4 Application circuit

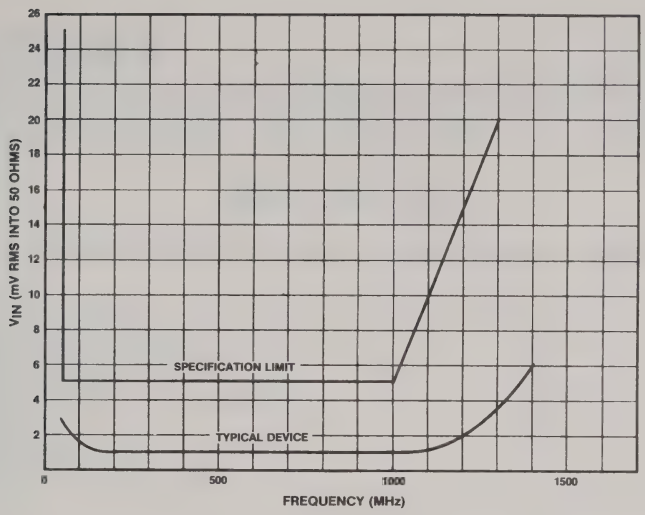

Fig.5 Typical input sensitivity

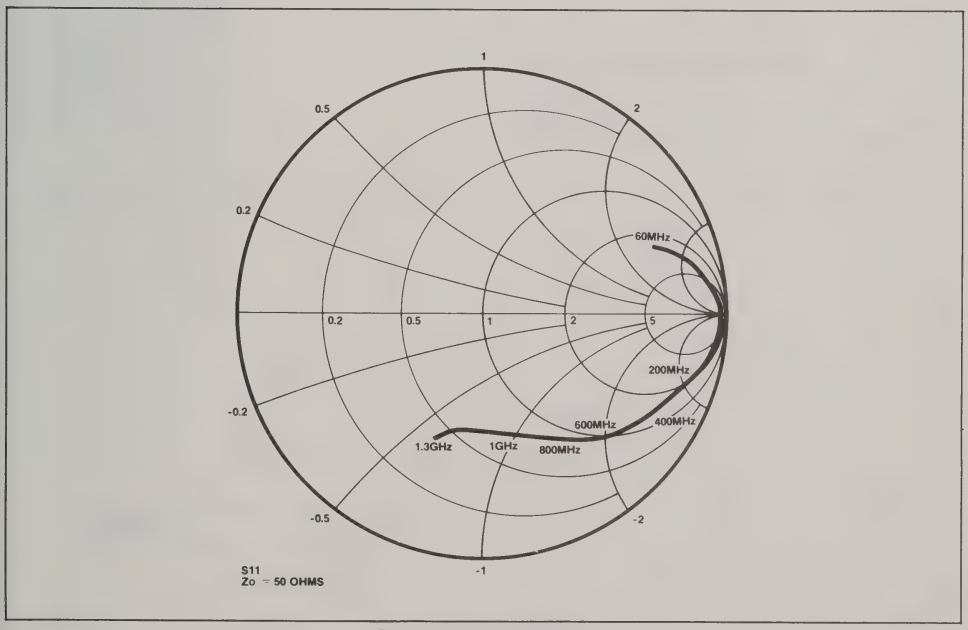

Fig.6 Typical input impedance

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SP4731 EXP

1.3GHz ÷ 64 HIGH OUTPUT SWING LOW CURRENT PRESCALER

The SP4731 ÷ 64 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. The device features a low supply current giving reduced dissipation and operating temperatures and is encapsulated in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4731 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL output.

Electrostatic protection is provided on all pins.

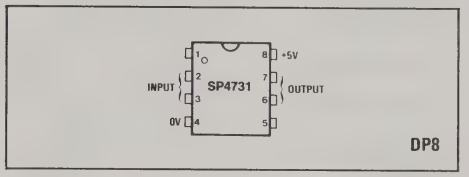

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- High Output Swing
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C

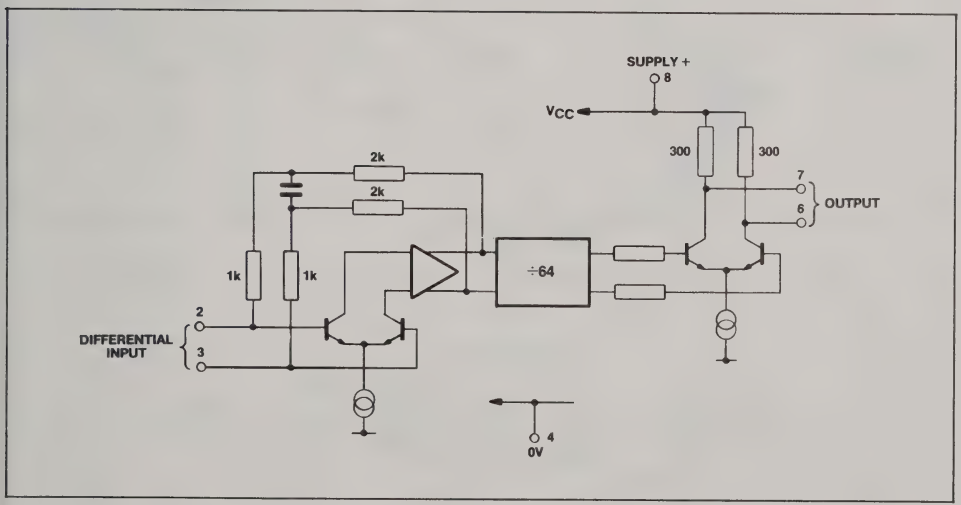

Fig.2 SP4731 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	Vcc = 5V
Input sensitivity	2,3					RMS sinewave (50 ohms system)
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.5
			2		pF	
Output voltage no load	6	1.0			V p-p	fin = 1.3GHz Vcc = 5V
	7	1.0			V p-p	
Output voltage load as Fig.3	6	tbd			V p-p	fin = 1.3GHz Vcc = 5V
	7	tbd			V p-p	
Output impedance	6		0.3		kohms	
	7		0.3		kohms	
Output imbalance	6,7			0.1	V	

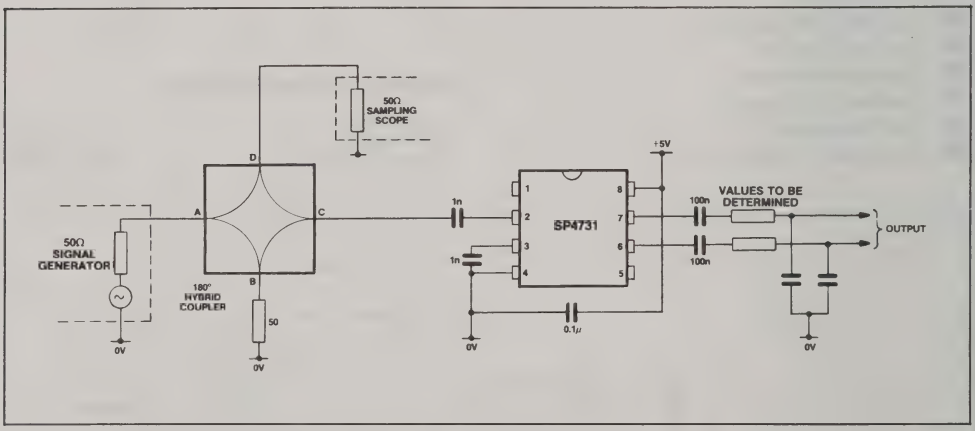

Fig.3 Test circuit

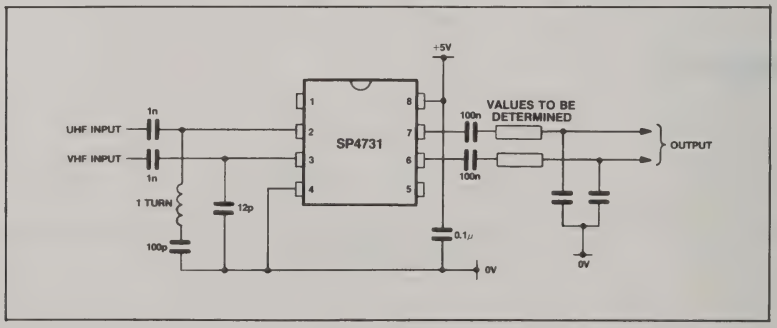

Fig.4 Application circuit

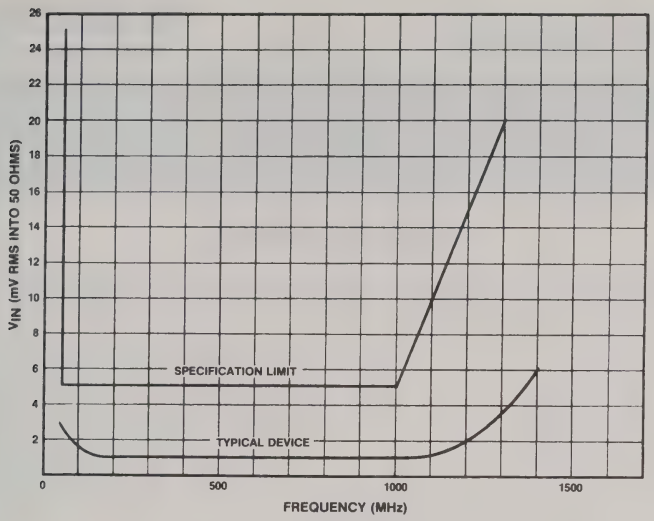

Fig.5 Typical input sensitivity

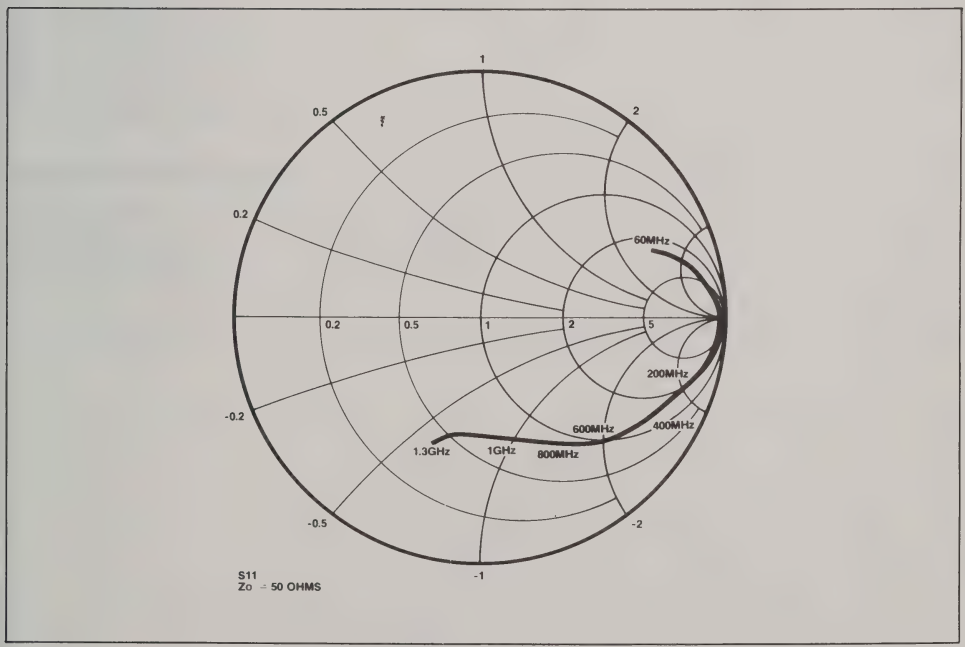

Fig.6 Typical input impedance

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SP4740 EXP

1.3GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4740 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4740 incorporates an on-chip preamplifier with differential inputs, and has a single TTL output.

Electrostatic protection is provided on all pins.

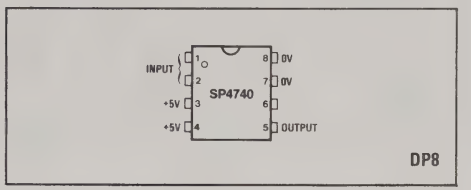

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- TTL Output
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C
Operating temperature range	0° C to +80° C

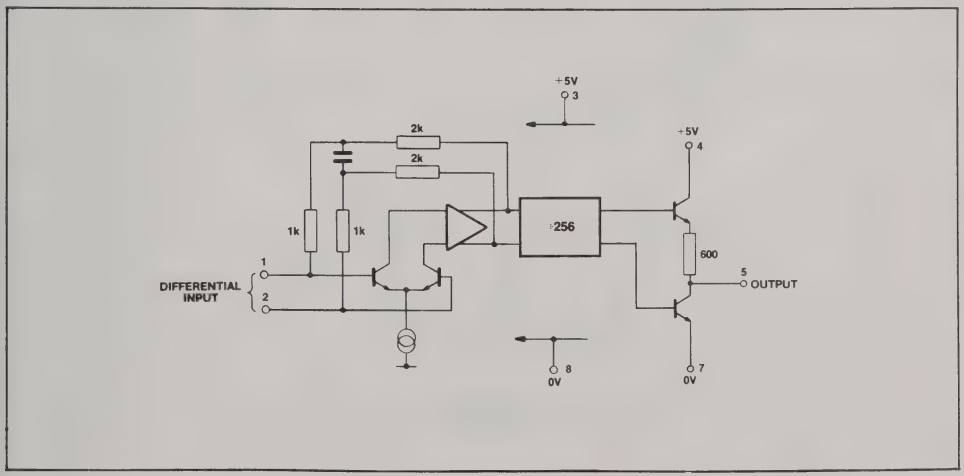

Fig.2 SP4740 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0° C to +70° C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply-current	8		35	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage						
High	5	3.3			V	Sourcing 0.2mA
Low	5			0.4	V	Sinking 2mA

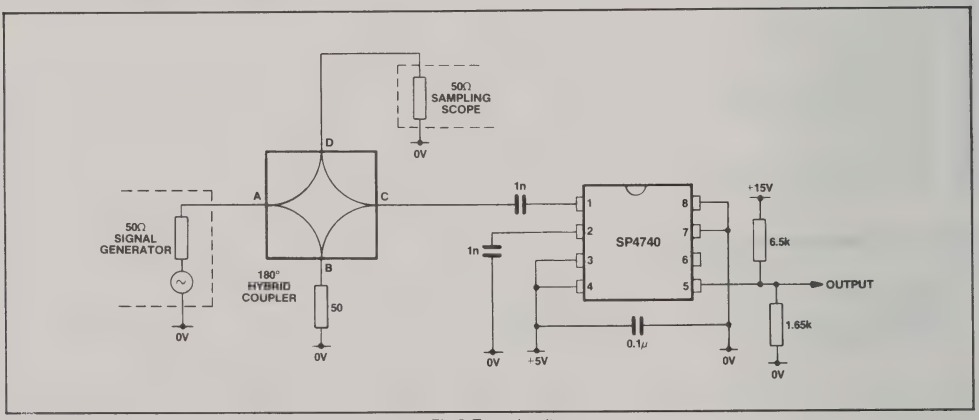

Fig.3 Test circuit

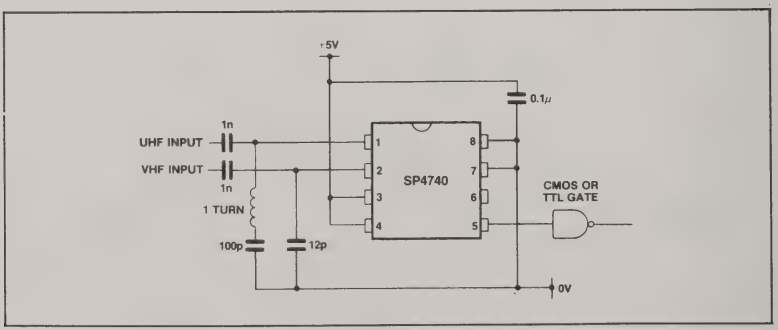

Fig.4 Application circuit

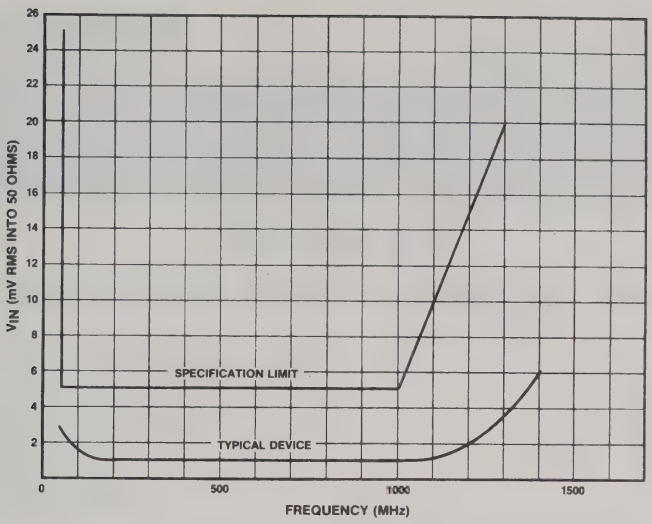

Fig.5 Typical input sensitivity

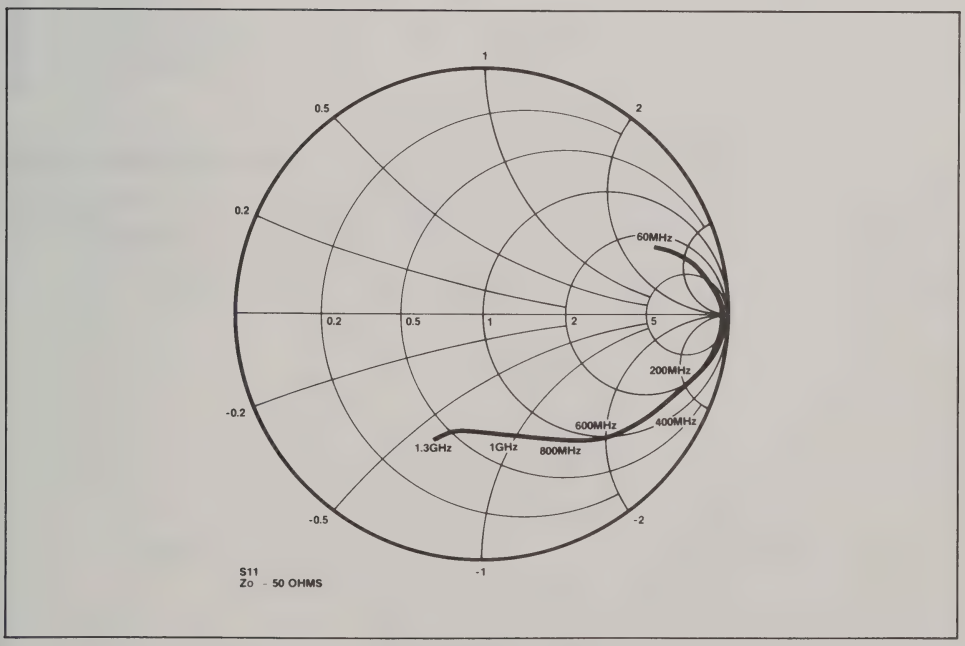

Fig.6 Typical input impedance

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SP4742 EXP

1.3GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4742 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. It has a lower supply current giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4742 incorporates an on-chip preamplifier with differential inputs, and has a single TTL output.

The device is specified to 1.3GHz.

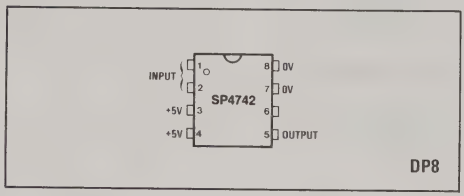

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- TTL Output

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55° C to +125° C

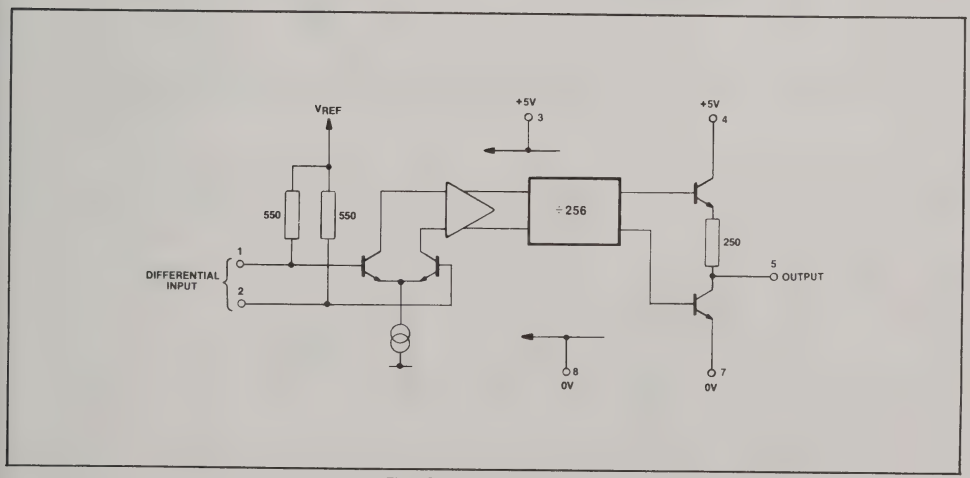

Fig.2 SP4742 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C, V_{CC} = 4.5V to 5.5V (For test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	3,4		25	35	mA	V_{CC} = 5V
Input sensitivity	1,2					RMS sinewave
50MHz			20	40	mV	
100MHz			8	15	mV	
200MHz			4	10	mV	
400MHz to 1000MHz			3	10	mV	
1200MHz			10	30	mV	
1300MHz			20	50	mV	
Input overload	1,2	300			mV	50MHz to 1.3GHz operating frequency
Input impedance	1,2		50		ohms	See Fig.6
			2		pF	
Output voltage						
High	5	3.3			V	Sourcing 0.2mA
Low	5			0.4	V	Sinking 2mA

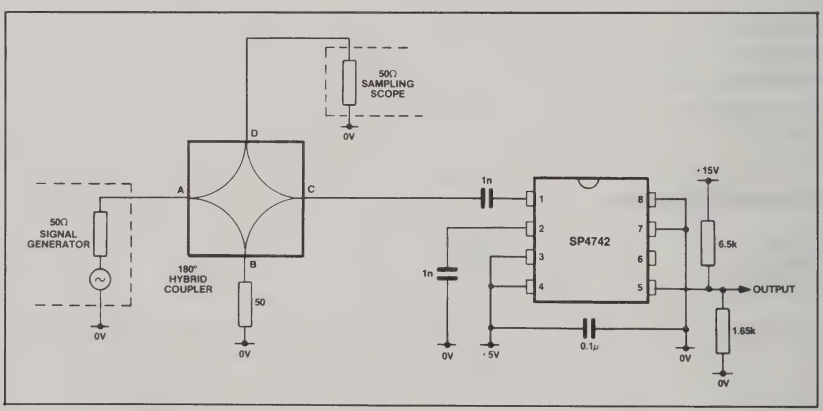

Fig.3 Test circuit

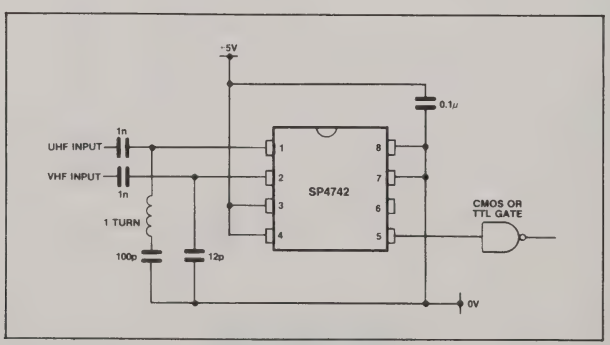

Fig.4 Application circuit

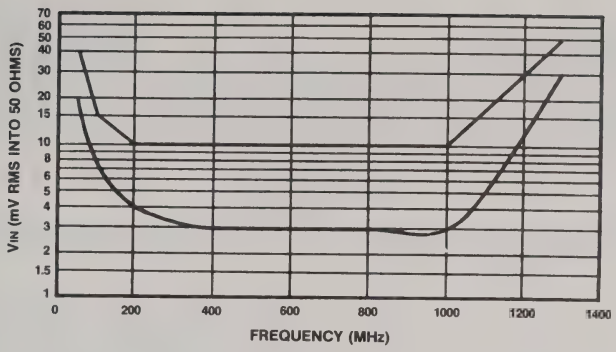

Fig.5 Typical input sensitivity

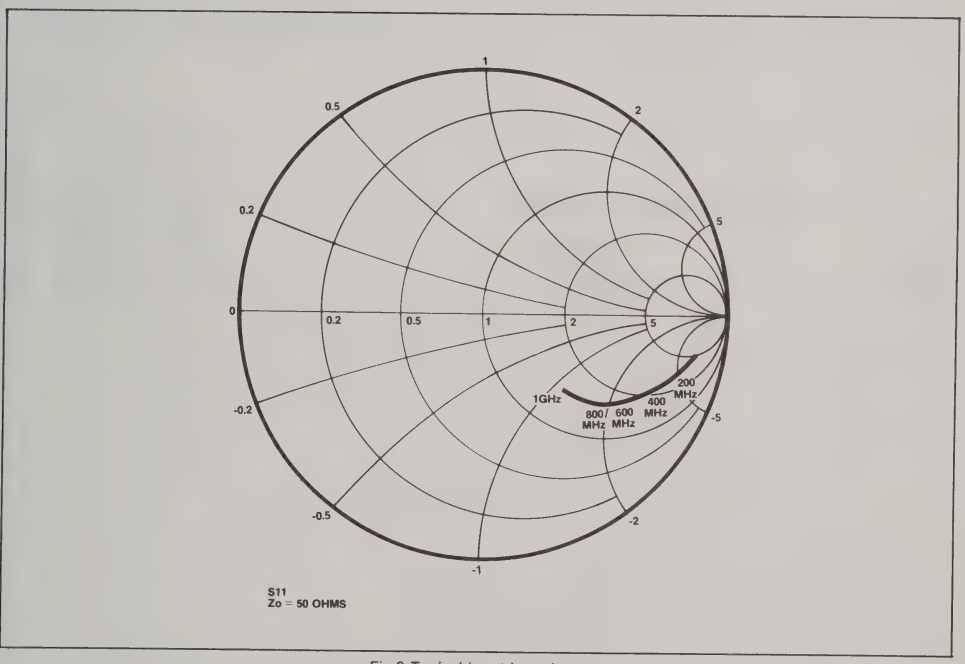

Fig.6 Typical input impedance

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SP4750

1.3GHz ÷ 256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4750 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. The device features a low supply current giving reduced dissipation and operating temperatures and is encapsulated in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4750 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL output.

Electrostatic protection is provided on all pins.

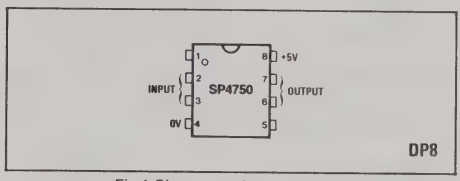

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C

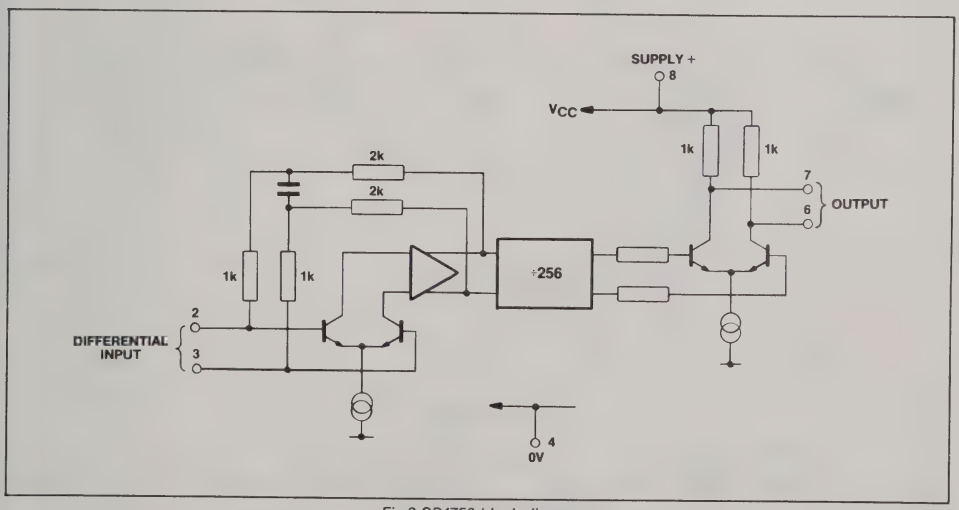

Fig.2 SP4750 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	0.8			V p-p	fin = 1.3GHz V_{CC} = 5V
	7	0.8			V p-p	fin = 1.3GHz V_{CC} = 5V
Output voltage load	6	0.6			V p-p	
as Fig.3	7	0.6			V p-p	
Output impedance	6		1		kohms	
	7		1		kohms	
Output imbalance	6,7			0.1	V	

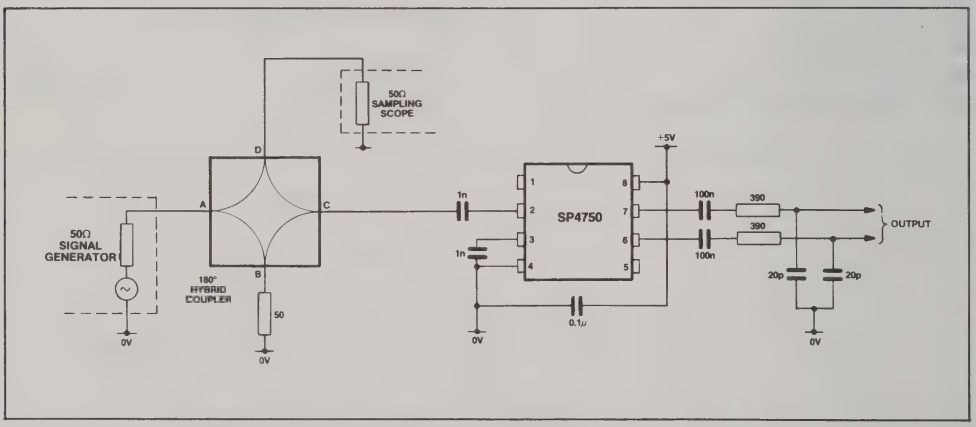

Fig.3 Test circuit

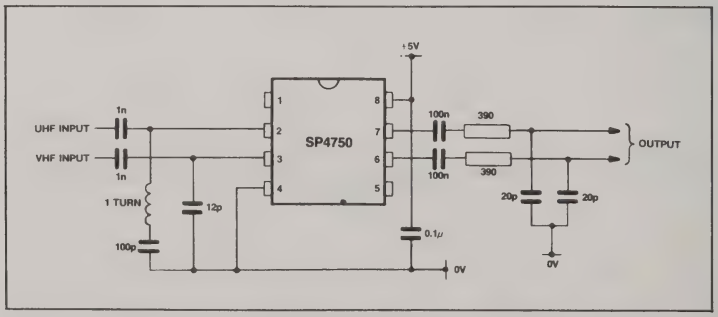

Fig.4 Application circuit

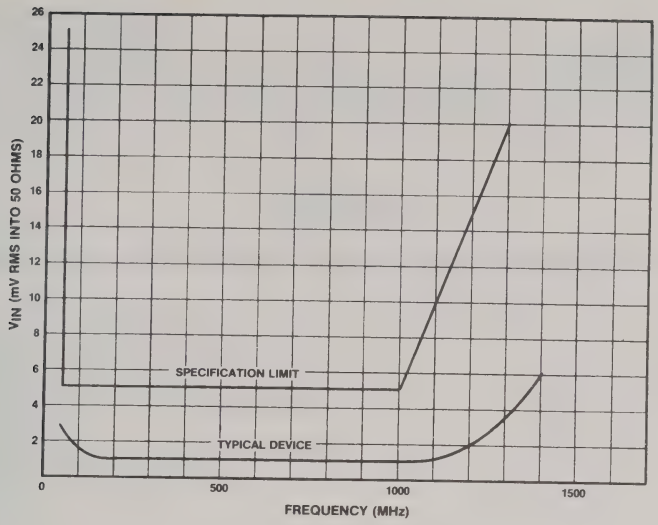

Fig.5 Typical input sensitivity

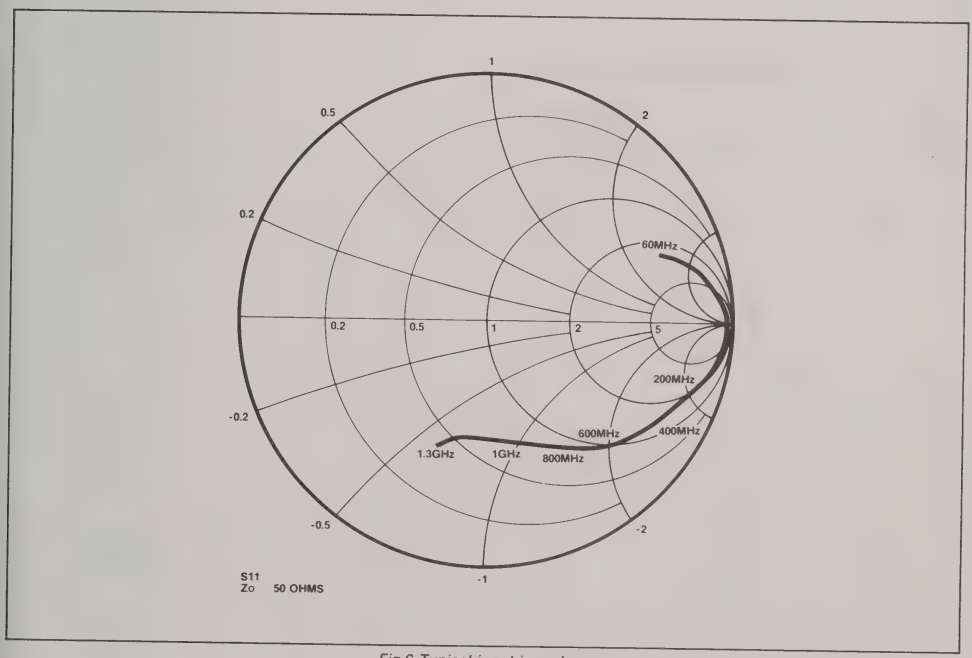

Fig.6 Typical input impedance

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SP4751

1.3GHz ÷ 256 HIGH OUTPUT SWING LOW CURRENT PRESCALER

The SP4751 ÷ 256 prescaler is one of Plessey Semiconductors' latest range of high speed dividers for consumer frequency synthesis and measurement systems. The device features a low supply current giving reduced dissipation and operating temperatures and is encapsulated in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4751 incorporates an on-chip preamplifier with differential inputs, and has balanced ECL output.

Electrostatic protection is provided on all pins.

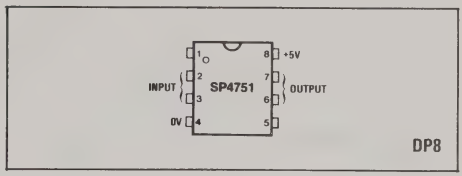

Fig.1 Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- High Output Swing
- Electrostatic Protection On Chip

ABSOLUTE MAXIMUM RATINGS

Supply voltage	V_{CC} +7V
Input voltage	2.5V p-p
Storage temperature	-55°C to +125°C

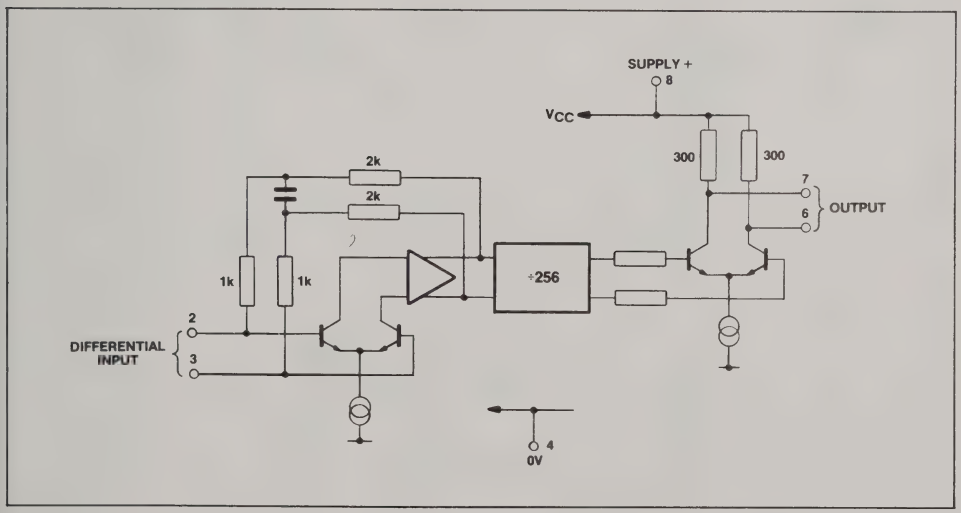

Fig.2 SP4751 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C V_{CC} = 4.5V to 5.5V (Test circuit see Fig.3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		35	50	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1.1GHz			1.5	10	mV	
1.2GHz			2	15	mV	
1.3GHz			4	20	mV	
Input overload	2,3	400			mV	50MHz to 500MHz
		300			mV	500MHz to 1.3GHz
Input impedance	2,3		50		ohms	See Fig.6
			2		pF	
Output voltage no load	6	1.0			V p-p	fin = 1.3GHz V_{CC} = 5V
	7	1.0			V p-p	
Output voltage load	6	t_{bd}			V p-p	fin = 1.3GHz V_{CC} = 5V
as Fig.3	7	t_{bd}			V p-p	
Output impedance	6		0.3		kohms	
	7		0.3		kohms	
Output imbalance	6,7			0.1	V	

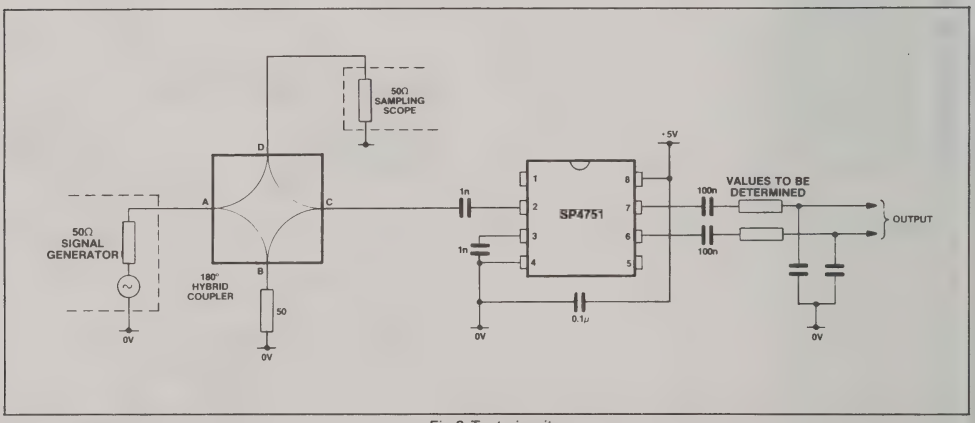

Fig.3 Test circuit

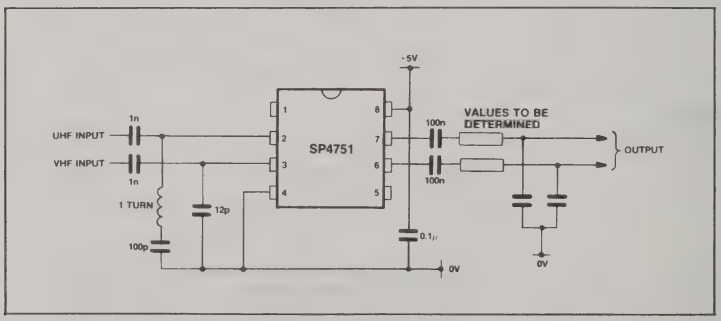

Fig.4 Application circuit

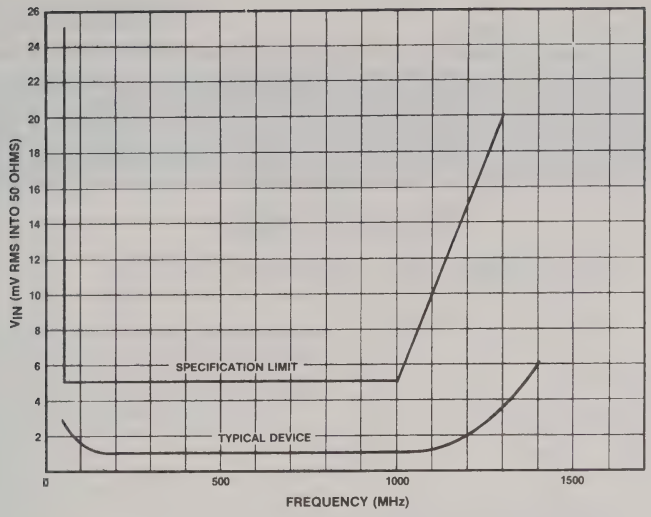

Fig.5 Typical input sensitivity

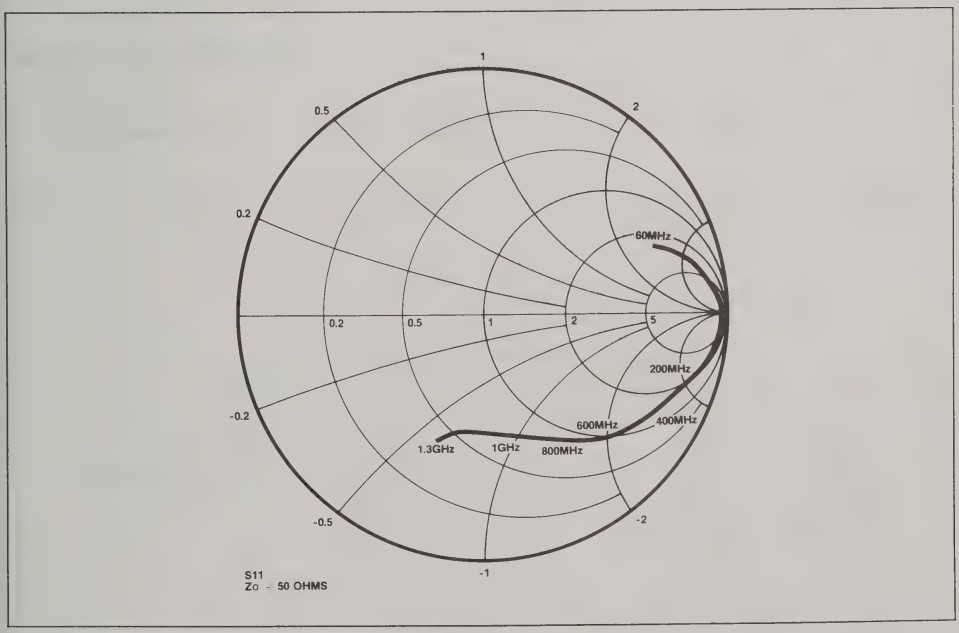

Fig.6 Typical input impedance

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SP4780 EXP

1.3GHz ÷4096 AND ÷8192 PRESCALER

The SP4780 is one of a new range of high speed dividers featuring low power consumption, high input sensitivity and low radiation.

The device, which is contained in an 8-pin minidip package has both ÷4096 and ÷8192 outputs available.

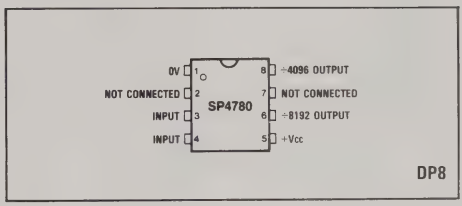

Fig.1 Pin connections top view

FEATURES

- Low Supply Current
- Low Radiation
- Specified to 1.3GHz
- High Input Sensitivity
- High Input Impedance

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc	+7V
Input Voltage	2.5V p-p
Storage Temperature	-55° C to +125° C

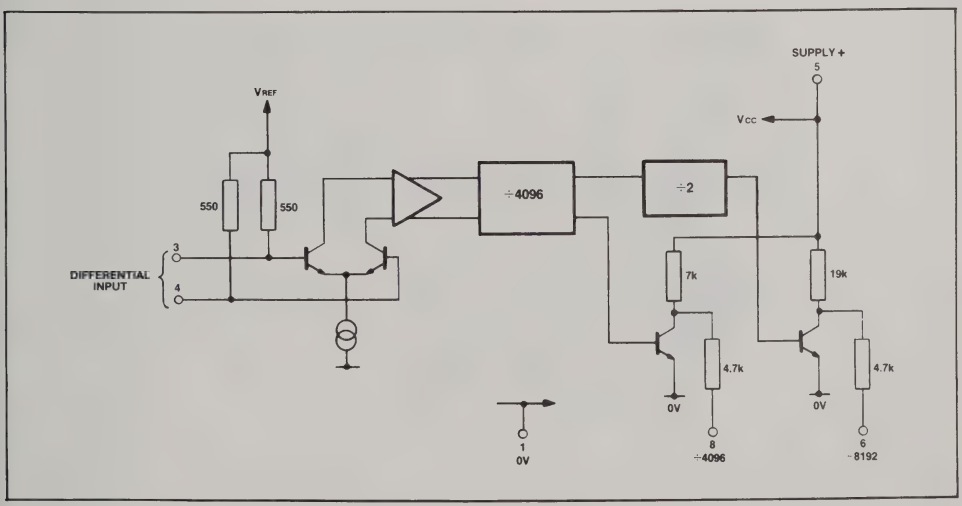

Fig.2 SP4780 block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C; V_{CC} = 4.5V to 5.5V (For test circuit see Fig.4)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	5		26	36	mA	V_{CC} = 5V
Input sensitivity	3,4					RMS sinewave
50MHz			20	40	mV	
100MHz			8	15	mV	
200MHz			4	10	mV	
400MHz			3	10	mV	
600MHz			3	10	mV	
800MHz			3	10	mV	
1000MHz			3	10	mV	
1200MHz			10	25	mV	
1300MHz			20	50	mV	
Input overload	3,4	300			mV	50MHz to 1.3GHz operating frequency
Input impedance (series equivalent)	3,4		50		Ω	See Fig.6
			2		pF	
Output voltage						
High		V_{CC}-0.5			V	With 8pF load
Low				0.5	V	fin = 1.3GHz
						V_{CC} = 5V
Output impedance	6		5		KΩ	Logic level '0'
	8		5		KΩ	
	6		24		KΩ	Logic level '1'
	8		12		KΩ	

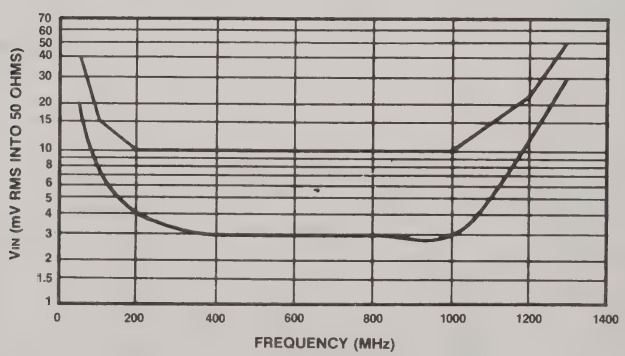

Fig.3 Typical input sensitivity

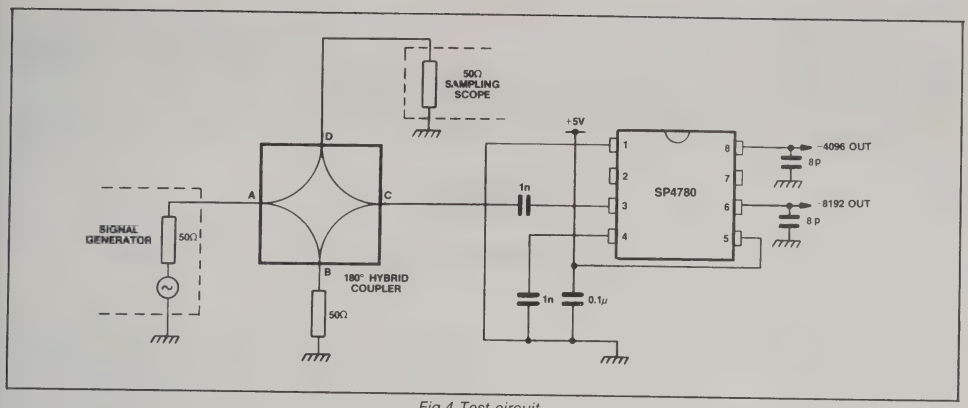

Fig.4 Test circuit

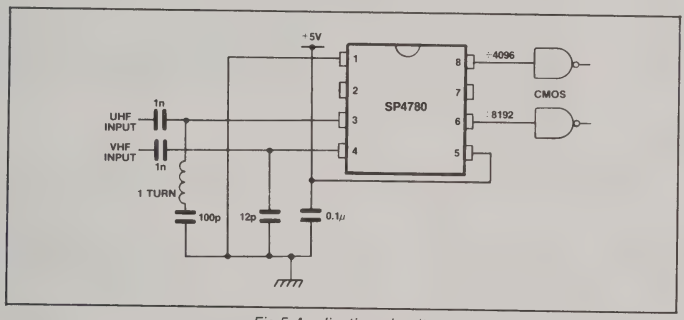

Fig.5 Application circuit

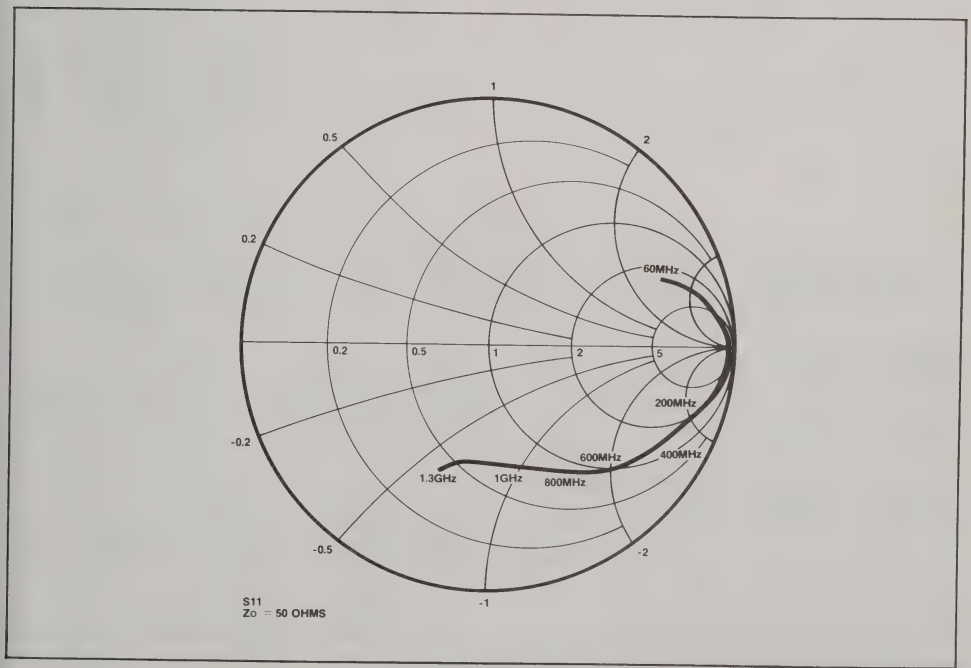

Fig.6 Typical input impedance

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SP5000

SINGLE CHIP FREQUENCY SYNTHESISER FOR TV TUNING

The SP5000, used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-16 prescaler with its own preamplifier and a 14 bit programmable divider controlled by a serially-loaded data register. Band selection lines are also included and give 4 switch output combinations on 3 lines. The frequency/phase comparator is fed with a 3.90625kHz reference, derived from the 4MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete Single Chip System for Microprocessor Control
- Operating Supply 5V, 60mA
- Prescaler and Preamplifier Included
- Single Port 16-bit Serial Data Entry
- Frequencies up to 1024MHz in 62.5kHz Steps (with 4.0MHz Ref)
- High Comparator Frequency Simplifies Charge Pump Filter
- Frequency Band Select Outputs
- Charge Pump Amplifier with Feedback and Disable
- Crystal Controlled Output Clock at 62.5kHz

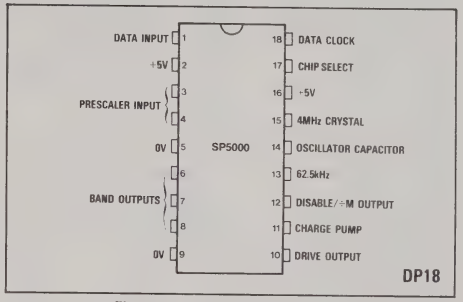

Fig.1 Pin connections - top view

Band select data		Band outputs Pin		
2^{15}	2^{14}	6	7	8
0	0	H	H	H
0	1	H	L	H
1	0	L	H	H
1	1	H	H	L

Table 1 Band select decoding

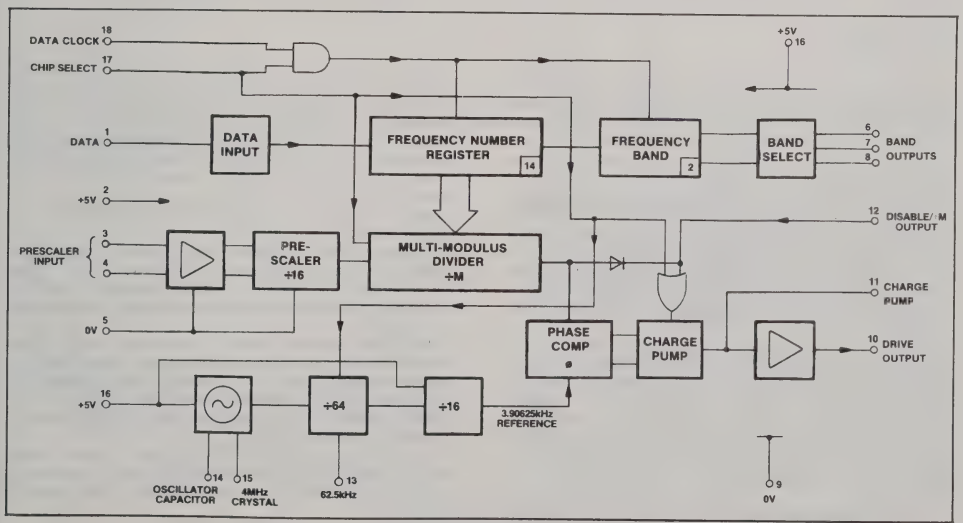

Fig.2 SP5000 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25° C, V_{CC} = 5V, Frequency standard = 4MHz

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	2,16	4.5		5.5	V	
Supply current	I_{CC} (2)	2		50	65	mA	
Supply current	I_{CC} (16)	16		1		mA	
Prescaler input voltage		3,4	17.5		200	mV	80MHz to 1GHz sinewave. See Fig.4
Prescaler input impedance		3,4		50		Ω	See Fig.5
High level input voltage		1,12,17,18	3.5		V_{CC}	V	
Low level input voltage		1,12,17,18	0		1.5	V	
High level input current		1,12,17			0.4	mA	V_{IN} = 5V
Input current		18			5	μA	V_{IN} = 3.5V
Multi-modulus divider output swing		12		350		mV	6.8k to 0V. Provided for test purposes only
Data clock input hysteresis		18		0.6		V	
Data clock rate		18			0.5	MHz	
Data setup time	t_{setup}	1,18	0.5			μs	See Fig.3
Chip select timing	csd(pos)	17,18	0		tc	μs	See Fig.3
Chip select timing	csd(neg)	17,18	0.5			μs	See Fig.3
External oscillator input		14,15		250		mV	AC coupled
Charge pump output current		11	±75	±100	±125	μA	V Pin 11 = 2.0V
Charge pump output leakage		11			±1	μA	V Pin 11 = 2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		14,15		0.12		ppm/° C	Over 0° C to 65° C temperature range. IC variation only
Oscillator stability with supply voltage		14,15		0.25		ppm/V	V_{CC} = 4.5V to 5.5V
Charge pump drive output current	I_{OUT}	10	1			mA	V Pin 10 = 0.7V
Band output leakage current		6,7,8			5	μA	V Pins 6,7 and 8 = 13.5V
Band output current		6,7,8	1	1.3		mA	V_{OUT} = 12V
Clock output leakage current		13			5	μA	V Pin 13 = 5.5V
Clock output saturation voltage		13			0.5	V	I Pin 13 = 1mA

DESCRIPTION

The phase comparator reference frequency at 3.90625kHz is obtained by division of the 4MHz on chip crystal controlled oscillator frequency. An output at 62.5kHz for driving the SP5010 in cable TV applications is provided at Pin 13.

In order to achieve a high sensitivity at the tuner local oscillator pick off point, the divide-by-sixteen prescaler is preceded by a differential amplifier with inputs on Pins 3 and 4. A simple filter arrangement is necessary at the inputs to prevent loading by the unused oscillator output when operation at both UHF and VHF frequencies is required.

The divide-by-sixteen prescaler output drives the multi-modulus divider, which, when the loop is locked, produces an output, frequency and phase locked to the 3.90625kHz reference.

Synthesis of the complete range of frequencies required for both off air and cable TV reception is provided by varying the division ratio of the multi-modulus divider according to data applied from an external control system. The data, applied as a 16 bit serial word, is loaded using the data clock and select lines from the control system into a storage register with fourteen bits controlling the multi-modulus divider, and the remaining bits the band select outputs on Pins 6, 7 and 8.

Data from the serial input, Pin 1 is clocked into the storage register by the positive edge of the data clock waveform on Pin 18 when the chip select input on Pin 17 is high. The chip select input should be timed to go high during the low portion of the clock waveform otherwise a positive transition coincident with the select signal will be applied to the storage register clock possibly causing a misreading of the applied data.

Figure 3 and Table 1 show the data format and timing requirements.

A single external transistor driven from the charge pump output provides the 30V swing necessary on the tuner varicap input. To prevent unwanted frequency variations when data is being entered, the charge pump is disabled by chip select.

Pin 12 is a dual input/output pin, the normal function being to disable the charge pump when the input is taken high. The alternative output function is provided for test purposes only and allows the ÷M counter output to be monitored. This signal is available at low amplitude when Pin 12 is loaded to ground by a 6.8k resistor.

To improve stability the +5V and ground supplies to the chip are split and brought out to separate pins, it is therefore essential to connect all four supply pins for the device to operate.

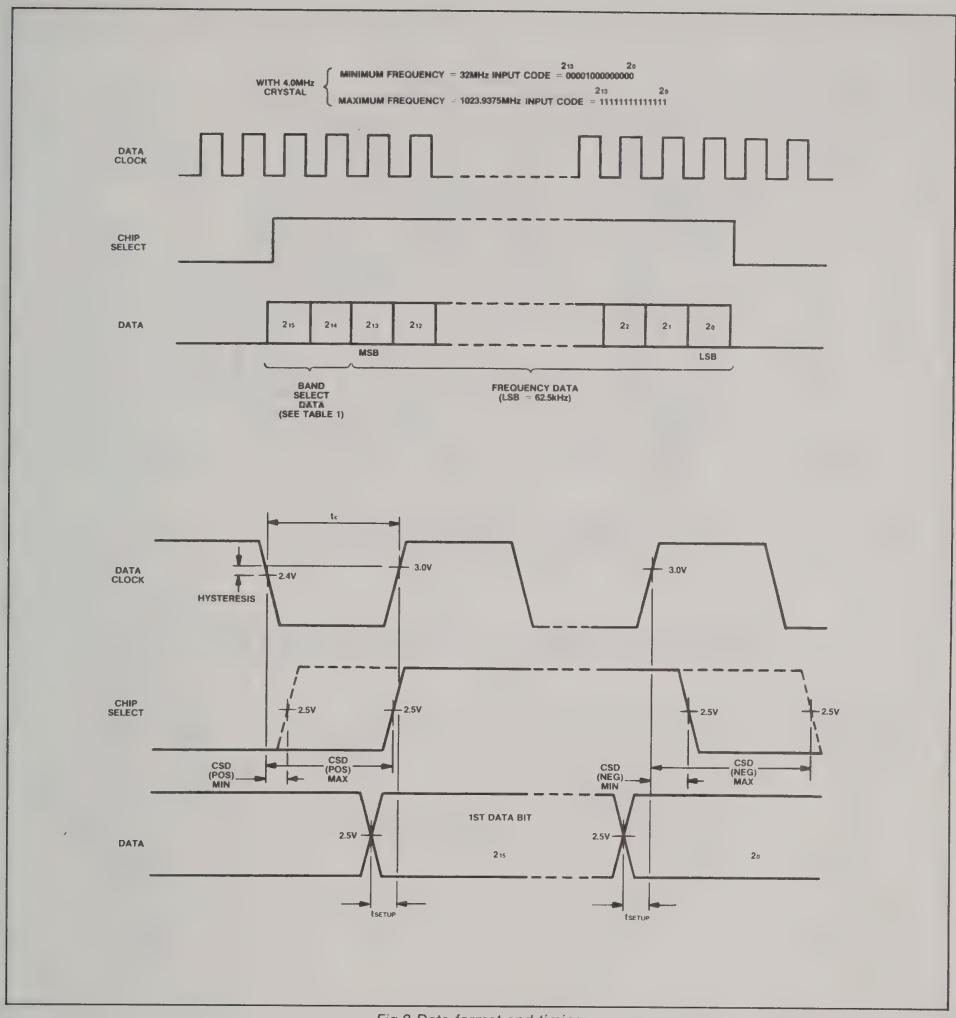

Fig.3 Data format and timing

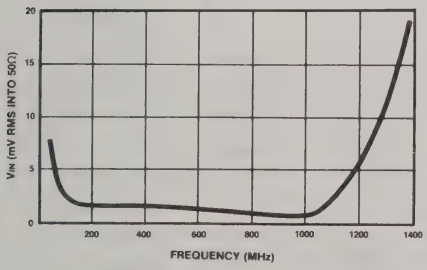

Fig.4 Typical input sensitivity of prescaler

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature: -10°C to +65°C
Storage temperature: -55°C to +125°C
Supply voltage Pin 2 and 16: 7V
Band select output voltage Pins 6,7,8: 14V
Prescaler input voltage: 2.5V p-p

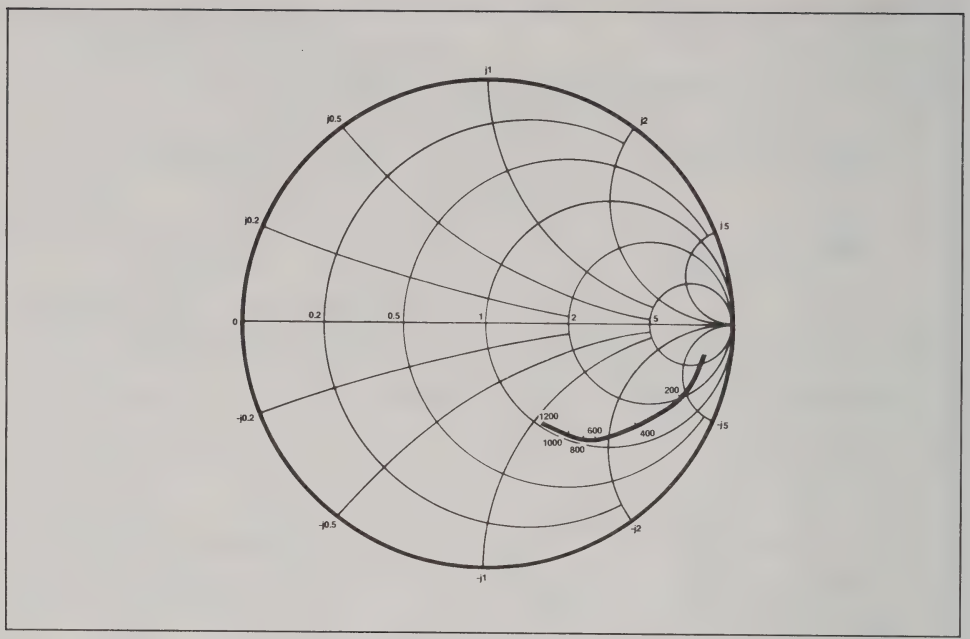

Fig.5 Typical input impedance frequencies in MHz. Normalised to 50 Ω

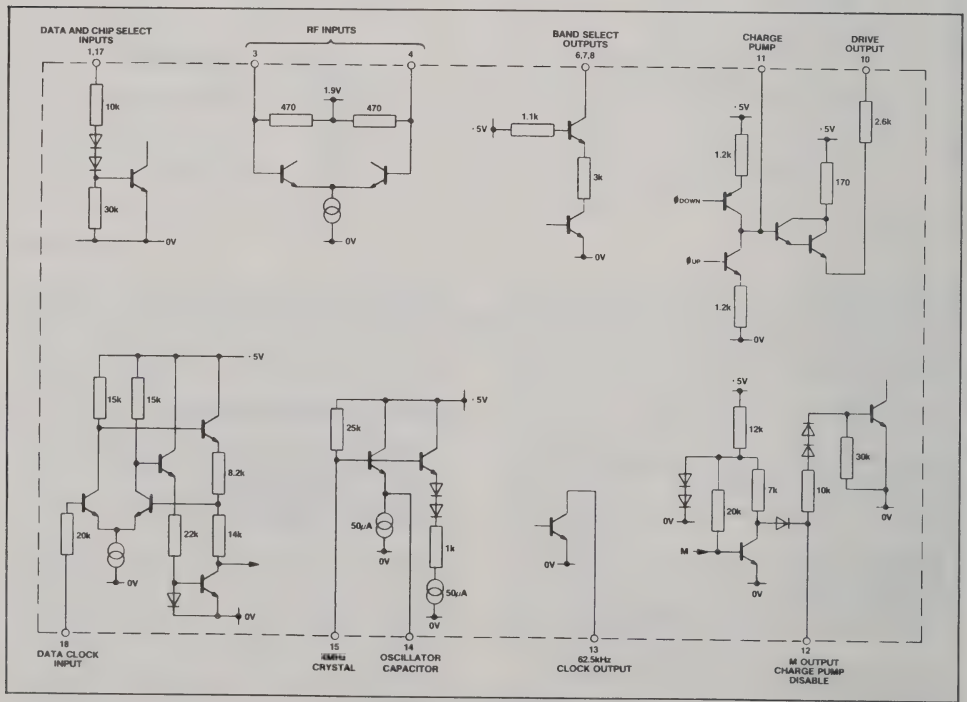

Fig.6 SP5000 input/output interface circuits

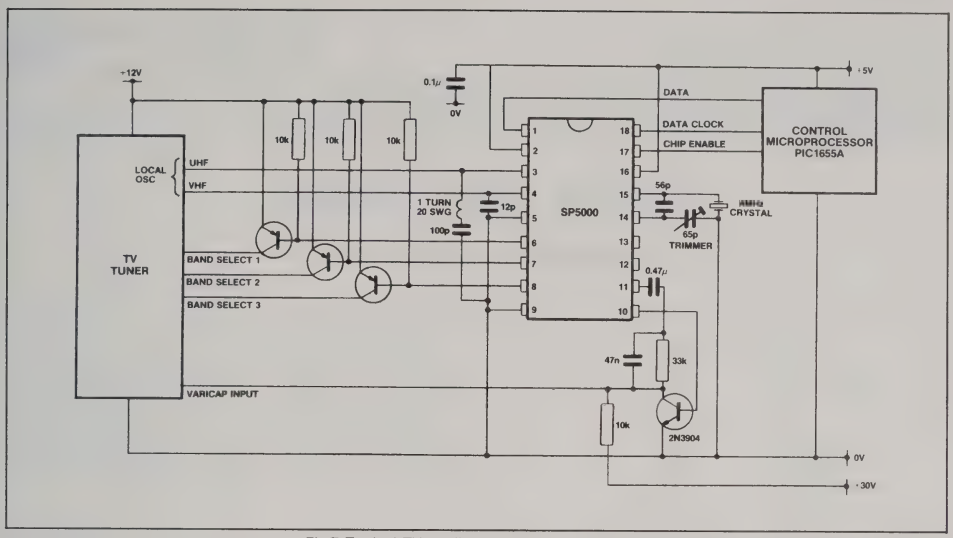

Fig.7 Typical TV application for 3 band reception

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SP5011 AND SP5012

CABLE TV PLL CONVERTERS

The SP5011/2 together with an appropriate voltage controlled oscillator (VCO), form a complete phase locked loop (PLL) synthesiser with 8-channel frequency selection. They consist of a prescaler with preamplifier and a divider programmable by means of link options on 3 pins. The frequency standard is derived from a 4MHz crystal controlled oscillator on-chip. A frequency/phase comparator working at 3.90625kHz feeds a charge pump output with an output amplifier stage around which a feedback filter may be applied.

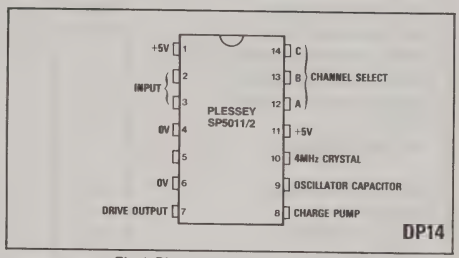

Fig.1 Pin connections - top view

FEATURES

- Complete 8-Channel System with Control
- +5V, 50mA Supply
- Prescaler and Preamplifier Included
- Frequencies Selected by Wire Links
- High Comparator Frequency for Easier Filtering
- Charge Pump Amplifier with Feedback Point
- 4MHz Crystal

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-10° C to +65° C
Storage Temperature	-55° C to +125° C
Supply Voltage Pin 1 and Pin 12	7V
Prescaler Input Voltage	2.5V p-p

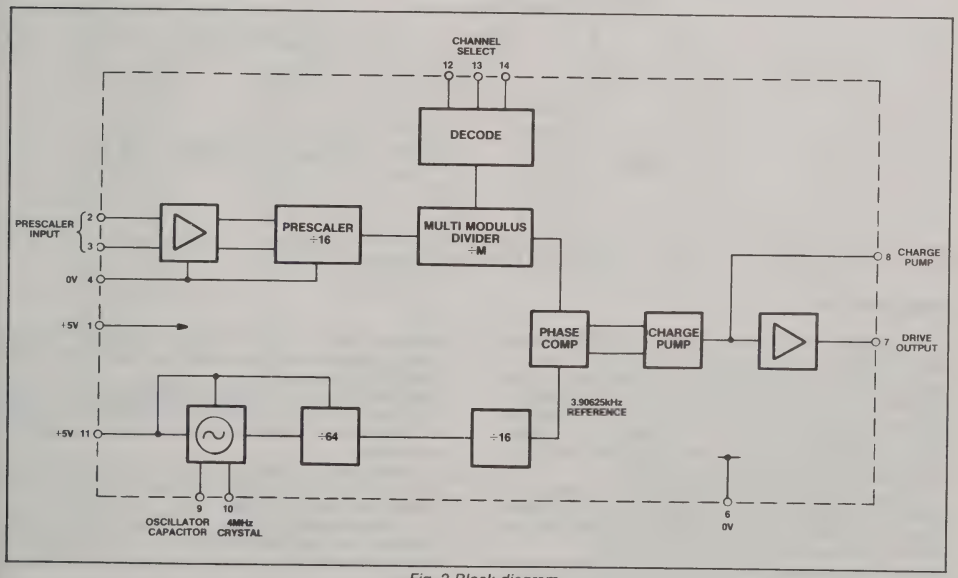

Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
T_{amb} = +25° C; V_{CC} = +5V

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	Vcc	1,11	4.5		5.5	V	
Supply current	Icc (1)	1		50	60	mA	
Supply current	Icc (11)	11		1		mA	
Prescaler input voltage		2,3	17.5		200	mV	RMS into 50Ω SP5011
Prescaler input voltage		2,3	10		200	mV	RMS into 50Ω SP5012
Prescaler input impedance		2,3		50		Ohms	
High level input voltage		12,13,14	3.5V		Vcc	V	
Low level input voltage		12,13,14	0		1.5	V	
High level input current		12,13,14			0.4	mA	V_{in} = 5V
Charge pump output current		8	±75	±100	±125	μA	V pin 8 = 2.0V
Charge pump leakage current		8			±1	μA	V pin 8 = 2.0V
Charge pump drive output current		7	1			mA	V pin 7 = 0.7V
Drift due to leakage				5		mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		9,10		0.12		PPM/° C	Over 0 to 65° C temperature range IC variation only
Oscillator stability with supply voltage		9,10		0.25		PPM/V	Vcc = 4.5V to 5.5V

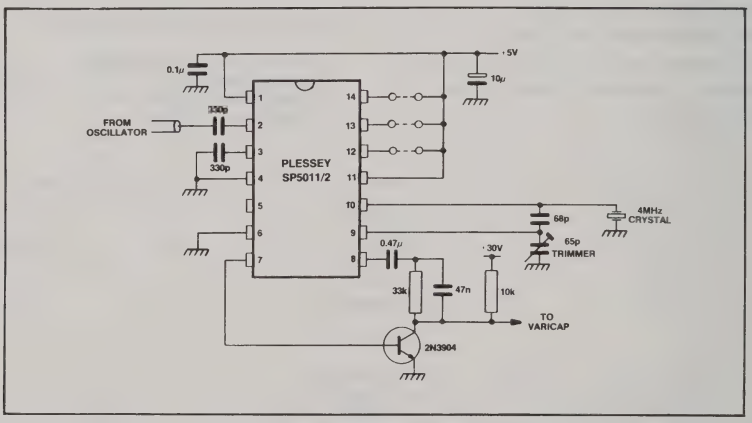

Fig.3 Typical application and test circuit

DESCRIPTION

The SP5011/2 when used with a voltage controlled oscillator form complete phase locked loop frequency synthesisers. Eight possible output frequencies are selectable by three wire links on each device. The SP5011 is intended to synthesise the 2nd LO frequency in American cable TV convertors using an IF frequency of 612.75MHz. The SP5012 will synthesise the vision carrier frequencies for European UHF channels as shown in Table 1.

A phase comparator reference frequency of 3.90625kHz is obtained by division of a 4MHz reference frequency which may be generated on chip or applied externally from the SP5000 reference oscillator where this is used.

In order to achieve a high sensitivity at the local oscillator pick off point the divide by sixteen prescaler is preceded by a differential amplifier with inputs on pins 2 and 3. The prescaler output is further divided by the multi-modulus divider, producing an output which is phase locked to the 3.90625kHz reference.

By changing the code on the channel select inputs on pins 12, 13 and 14 the division ratio of the multi-modulus divider can be changed to allow synthesis of eight local oscillator frequencies.

A single external transistor driven from the charge pump output provides the output swing necessary for the local oscillator varicap control line.

To improve device stability the +5V and ground supplies to the chip are split and brought out to separate pins. It is therefore essential to connect all supply pins for the device to operate.

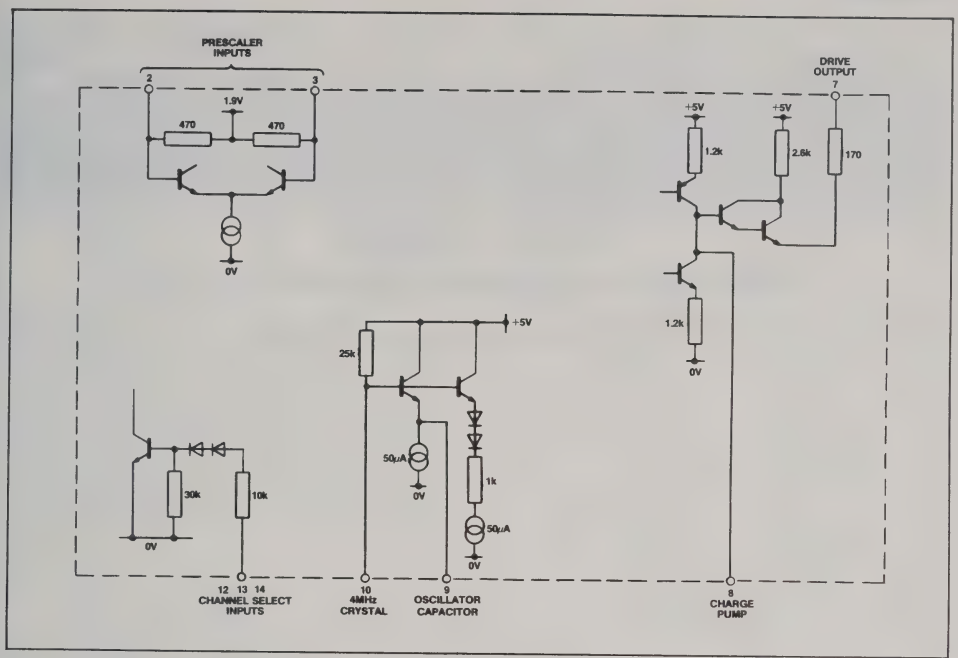

Fig.4 SP5011/2 input/output interface circuits

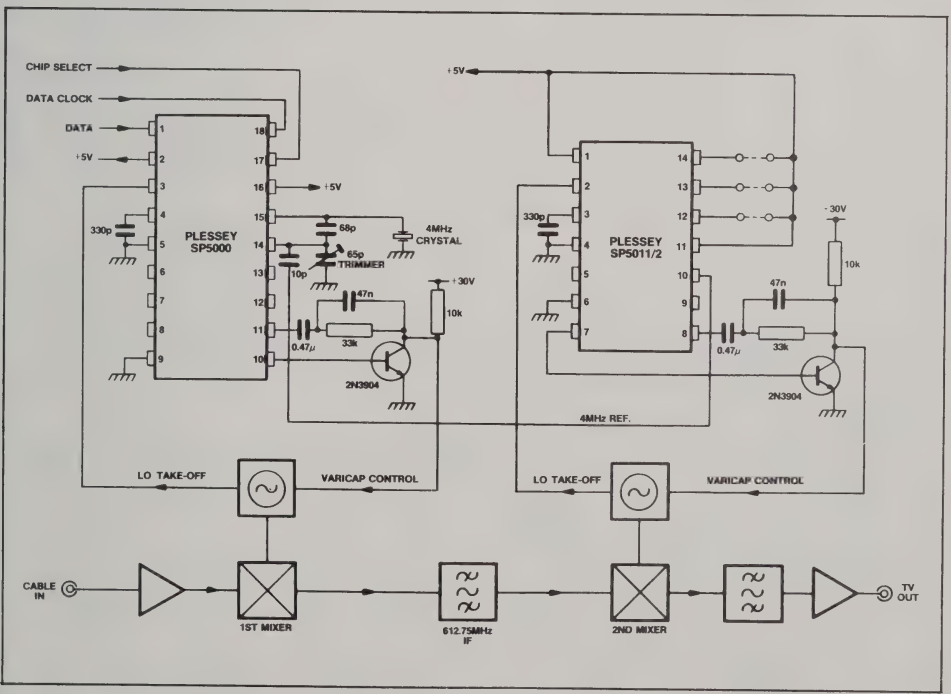

Fig.5 Cable TV set top converter

A Pin 12	B Pin 13	C Pin 14	SP5011 (2nd IF frequency = 612.75MHz)			SP5012	
			USA channel	Synthesised frequency	Mixer output frequency	European UHF channel	Vision carrier frequency
0	0	0	5	690MHz	77.25MHz	24	495.25MHz
0	0	1	6	696MHz	83.25MHz	25	503.25MHz
0	1	0	3 vision carrier	61.25MHz	-	32	559.25MHz
0	1	1	4 vision carrier	67.25MHz	-	33	567.25MHz
1	0	0	3	674MHz	61.25MHz	34	575.25MHz
1	0	1	2	668MHz	55.25MHz	35	583.25MHz
1	1	0	4	680MHz	67.25MHz	36	591.25MHz
1	1	1	TV IF	567MHz	45.75MHz	37	599.25MHz

Table 1 Channel selection coding for SP5011 and SP5012

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SP5050/1 EXP

1.8/2GHz SINGLE CHIP FREQUENCY SYNTHESISER

The SP5050/1, used with a voltage controlled oscillator, forms a complete phase locked loop system. The circuit consists of a divide-by-32 prescaler with its own preamplifier and a 14 bit programmable divider controlled by a serially-loaded data register. Control selection lines are also included and give 4 switch output combinations on 3 lines. The frequency/phase comparator is fed with a 3.90625kHz reference, derived from the 4 MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete Single Chip System for Microprocessor Control
- Operating Supply 5V, 90mA/70mA
- Prescaler and Preamplifier Included
- Single Port 16-Bit Serial Data Entry
- Frequencies up to 2048MHz in 125kHz Steps (with 4.0MHz Ref)
- High Comparator Frequency Simplifies Charge Pump Filter
- 3 Selectable Control Outputs Are Available
- Charge Pump Amplifier with Feedback and Disable
- Crystal Controlled Output Clock at 62.5kHz

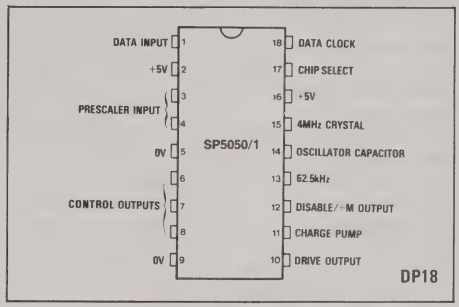

Fig.1 Pin connections - top view

Control select data		Control outputs Pin		
2^{15}	2^{14}	6	7	8
0	0	H	H	H
0	1	H	L	H
1	0	L	H	H
1	1	H	H	L

Table 1 Control select decoding

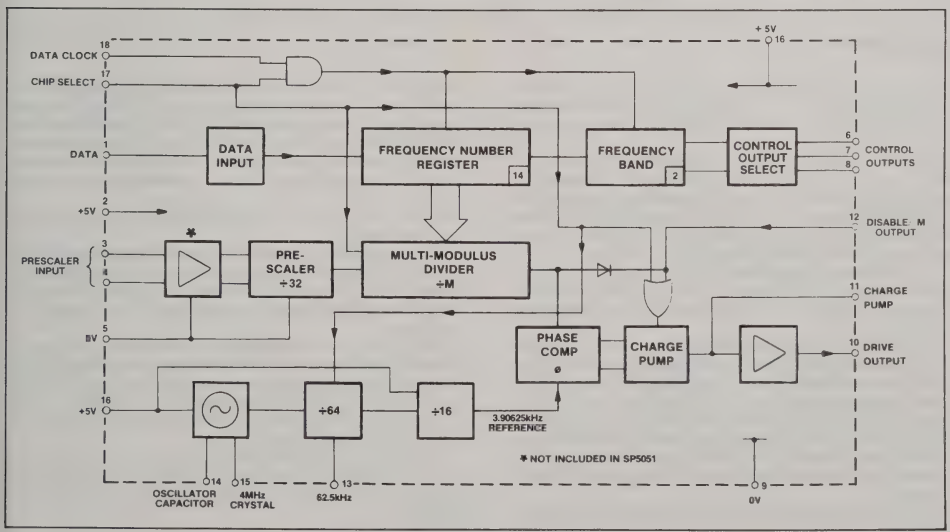

Fig.2 SP5050/1 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25° C, V_{CC} = 5V, Frequency standard = 4MHz

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	2,16	4.5		5.5	V	
Supply current	I_{CC}	2		85		mA	SP5051
Supply current	I_{CC}	2		70		mA	SP5050
Prescaler input voltage		3,4	50			mV	300MHz to 1.8GHz sinewave - SP5050
		3,4	100			mV	See Fig.4,5 - SP5051
Prescaler input impedance		3,4		50		Ω	See Fig.6
High level input voltage		1,12,17,18	3.5		V_{CC}	V	
Low level input voltage		1,12,17,18	0		1.5	V	
High level input current		1,12,17			0.4	mA	V_{IN} = 5V
Input current		18			5	μA	V_{IN} = 3.5V
Multi-modulus divider output swing		12		350		mV	6.8k to 0V. Provided for test purposes only
Data clock input hysteresis		18		0.6		V	
Data clock rate		18			0.5	MHz	
Data setup time	t_{setup}	1,18	0.5			μs	See Fig.3
Chip select timing	csd(pos)	17,18	0		tc	μs	See Fig.3
Chip select timing	csd(neg)	17,18	0.5			μs	See Fig.3
External oscillator input		14,15		250		mV	AC coupled
Charge pump output current		11	±75	±100	±125	μA	V Pin 11 = 2.0V
Charge pump output leakage		11			±1	μA	V Pin 11 = 2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		14,15		0.12		ppm/° C	Over 0° C to 65° C temperature range. IC variation only.
Oscillator stability with supply voltage		14,15		0.25		ppm/V	V_{CC} = 4.5V to 5.5V
Charge pump drive output current	I_{OUT}	10	1			mA	V Pin 10 = 0.7V
Control output leakage current		6,7,8			5	μA	V Pins 6,7 and 8 = 13.5V
Control output current		6,7,8	1	1.3		mA	V_{OUT} = 12V
Clock output leakage current		13			5	μA	V Pin 13 = 5.5V
Clock output saturation voltage		13			0.5	V	I Pin 13 = 1mA

DESCRIPTION

The phase comparator reference frequency at 3.90625kHz is obtained by division of the 4MHz on chip crystal controlled oscillator frequency. An outpt at 62.5kHz is provided at Pin 13.

In order to achieve a high sensitivity at the tuner local oscillator pick off point, the divide-by-32 prescaler is preceded by a differential amplifier with inputs on Pins 3 and 4. The SP5051 does not contain this preamp as it limits the frequency range. But as a consequence the SP5051 is not as sensitive as the SP5050 in the lower frequency region.

The divide-by-32 prescaler output drives the multi-modulus divider, which, when the loop is locked, produces an output, frequency and phase locked to the 3.90625kHz reference.

Synthesis of the complete range of frequencies from 64 MHz to 2048MHz is provided by varying the division ratio of the multi-modulus divider according to data applied from an external control system. The data,applied as a 16-bit serial word,is loaded using the data clock and select lines from the control system into a storage register with fourteen bits controlling the multi-modulus divider,while the remaining bits determine the control outputs on Pins 6,7 and 8.

Data from the serial input, Pin 1 is clocked into the storage register by the positive edge of the data clock waveform on Pin 18 when the chip select input on Pin 17 is high. The chip select input should be timed to go high during the low portion of the clock waveform otherwise a positive transition coincident with the select signal will be applied to the storage register clock possibly causing a misreading of the applied data.

Figure 3 and Table 1 show the data format and timing requirements.

A single external transistor driven from the charge pump output provides the 30V swing necessary on the oscillator varicap input. To prevent unwanted frequency variations when data is being entered, the charge pump is disabled by chip select.

Pin 12 is a dual input/output pin, the normal function being to disable the charge pump when the input is taken high. The alternative output function is provided for test purposes only and allows the ÷M counter output to be monitored. This signal is available at low amplitude when Pin 12 is loaded to ground by a 6.8k resistor.

To improve stability the +5V and ground supplies to the chip are split and brought out to separate pins, it is therefore essential to connect all four supply pins for the device to operate.

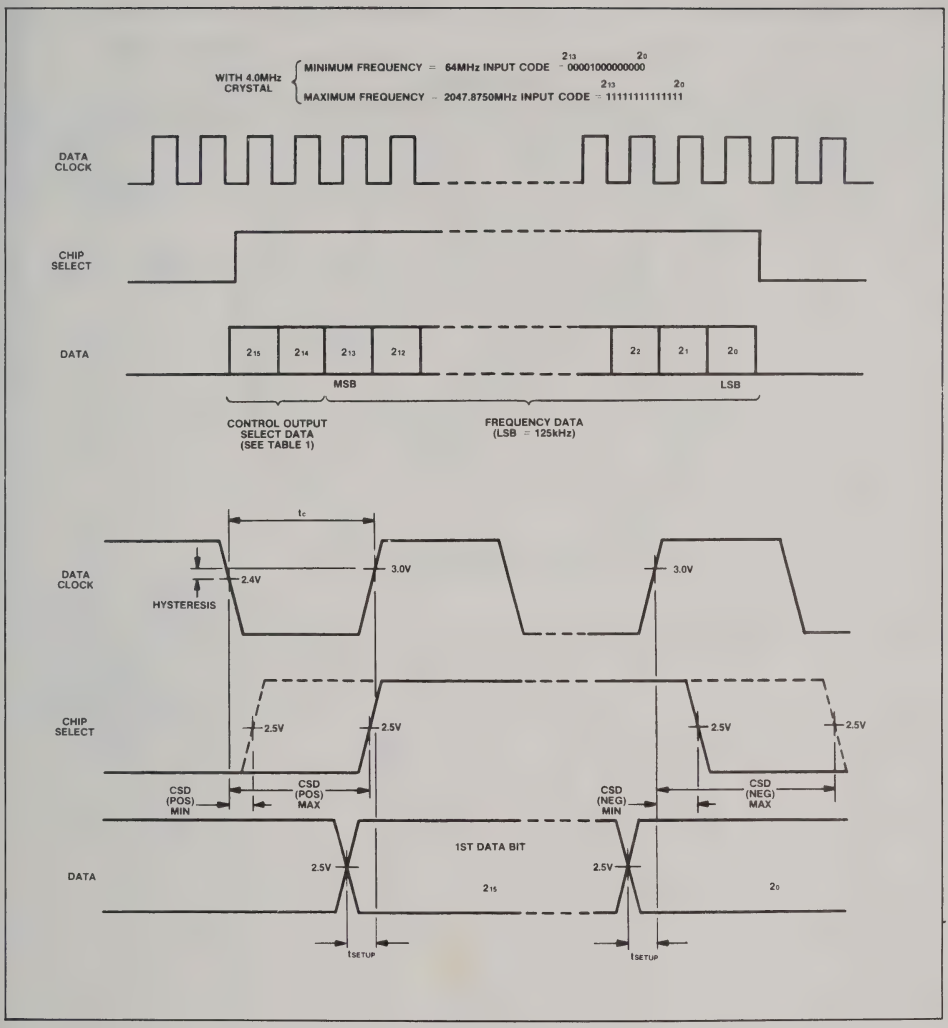

Fig.3 Data format and timing

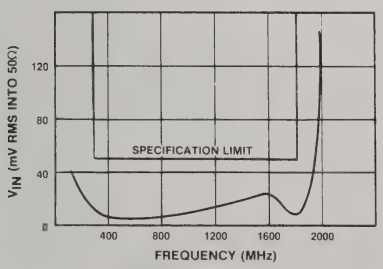

Fig.4 SP5050 typical input sensitivity

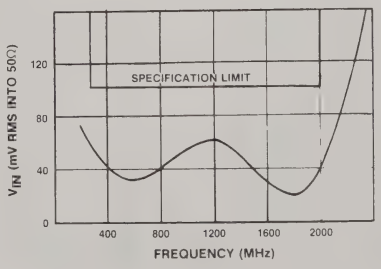

Fig.5 SP5051 typical input sensitivity

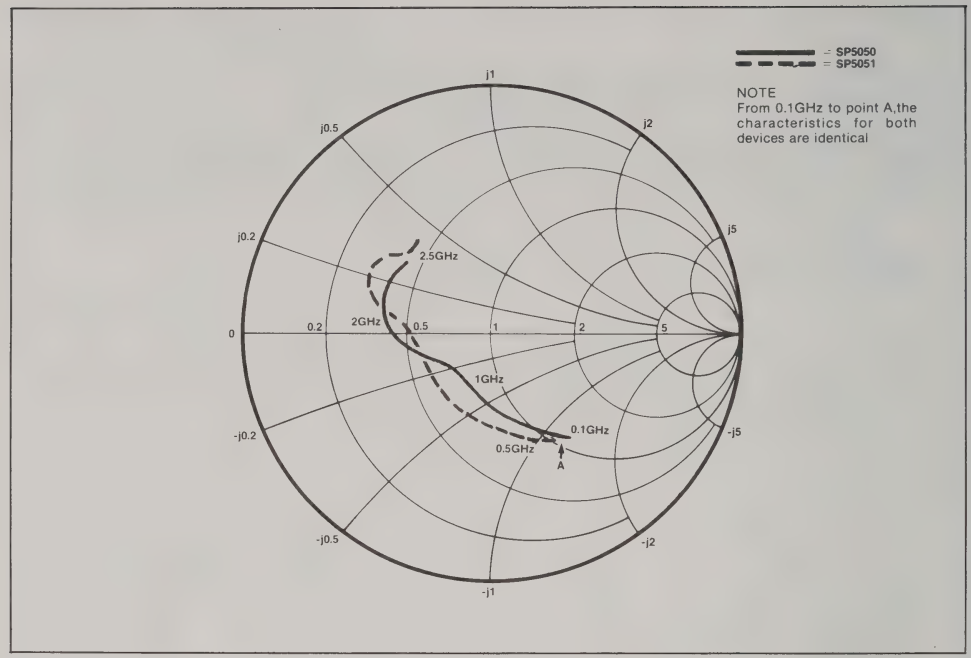

Fig.6 Typical input impedance frequencies in MHz. Normalised to 50Ω

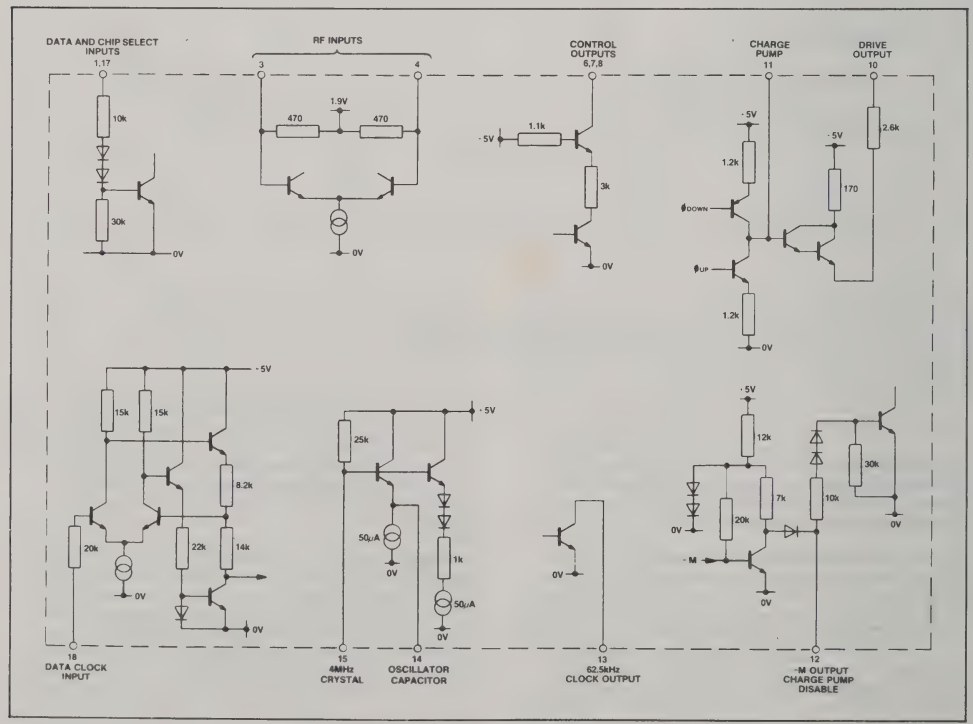

Fig.7 SP5050/1 input/output interface circuits

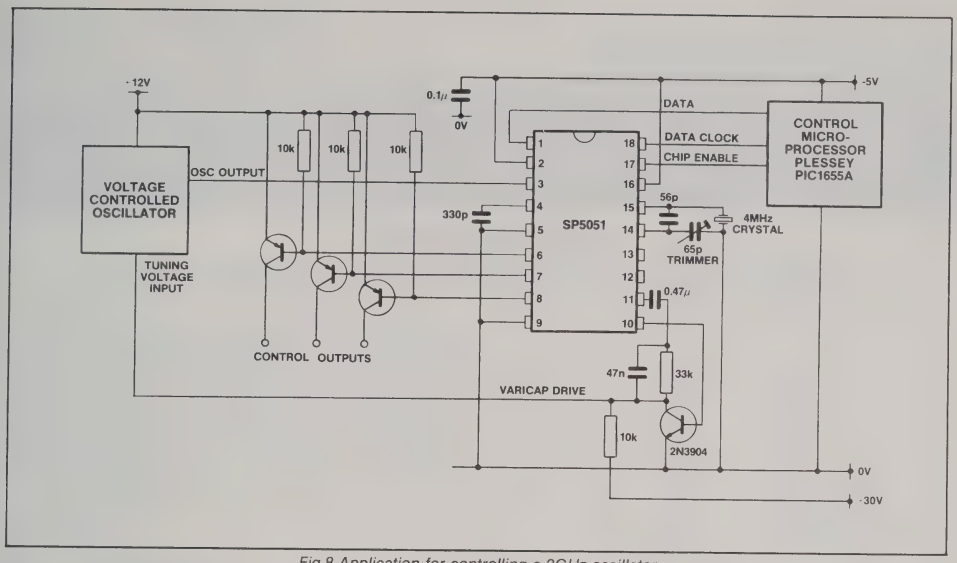

Fig.8 Application for controlling a 2GHz oscillator

ABSOLUTE MAXIMUM RATINGS

Ambient operating temperature	-10° C to +65° C
Storage temperature	-55° C to +125° C
Supply voltage Pin 2 and 16	7V
Band select output voltage Pins 6,7,8	14V
Prescaler input voltage	2.5V p-p

PLESSEY
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SP5060 EXP

1.8GHz FIXED MODULUS FREQUENCY SYNTHESISER

The SP5060 is for use in outdoor (head end) units of satellite TV receivers and together with an appropriate voltage controlled oscillator (VCO), forms a complete phase locked loop (PLL) synthesiser. The circuit consists of a prescaler with preamplifier and a fixed modulus divider. The phase comparator is fed with a reference frequency derived from an external oscillator or crystal. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

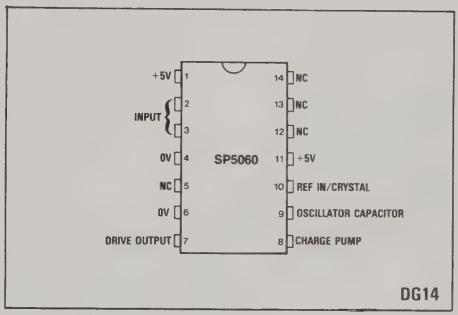

Fig.1 Pin connections - top view

FEATURES

- +5V, 50mA Supply
- Prescaler and Preamplifier Included
- High Comparator Frequency for Easier Filtering
- Charge Pump Amplifier with Feedback Point
- Synthesises Frequencies up to 1.8GHz
- For use at C-Band with Frequency Doubling Mixer

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	**-10°C to +70°C**
Maximum junction temperature	175°C
Storage temperature	-55°C to +125°C
Supply voltage Pin 1 and Pin 11	7V
Prescaler input voltage	2.5V p-p

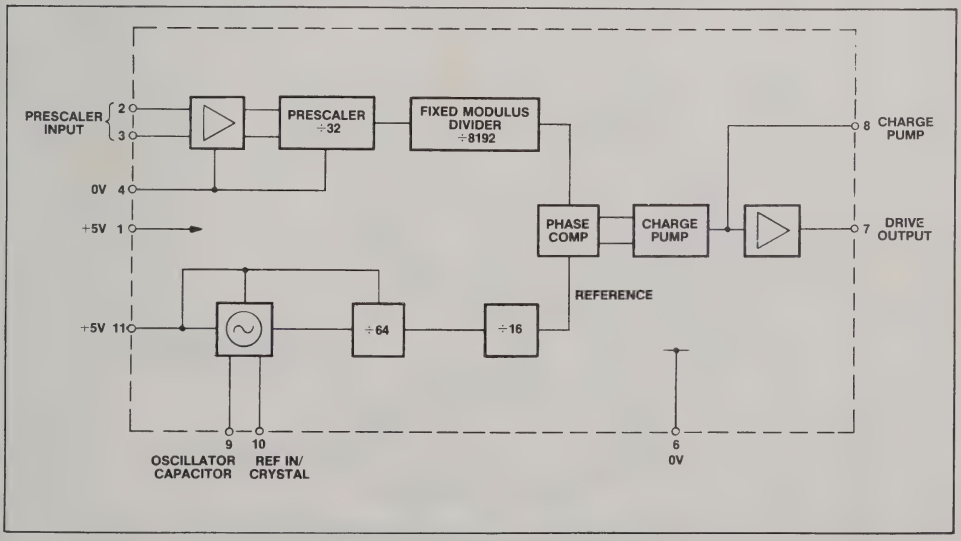

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C V_{CC} = +4.5V to 5.5V

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min.	Typ.	Max.		
Operating voltage	V_{CC}	1,11	4.5		5.5	V	
Supply current	$I_{CC}(1)$	1		50	60	mA	
Supply current	$I_{CC}(11)$	11		1		mA	
Prescaler input voltage		2,3	50			mV	300MHz to 1.8GHz sinewave
Prescaler input impedance		2,3		50		Ohms	
Charge pump output current		8	±75	±100	±125	μA	V pin 8 = 2.0V
Charge pump leakage current		8			±1	μA	V pin 8 = 2.0V
Charge pump drive output current		7	1			mA	V pin 7 = 0.7V
Drift due to leakage				5		mV/s	At collector of external varicap drive transistor
Oscillator temperature stability		9,10		0.12		PPM/°C	Over 0 to 65°C temperature range IC variation only
Oscillator stability with supply voltage		9,10		0.25		PPM/V	V_{CC} = 4.5V to 5.5V
Reference clock frequency		10	2		7.1	MHz	
External reference amplitude		10	100		500	mV rms	
Reference input impedance		10		25		kohms	

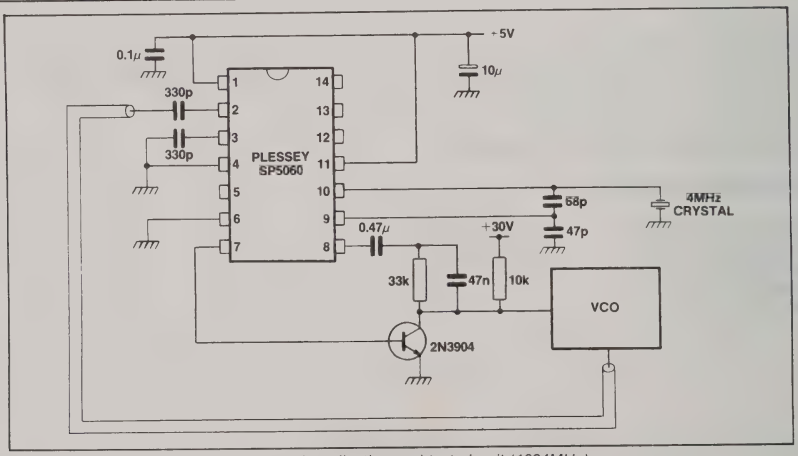

Fig.3 Typical application and test circuit (1024MHz)

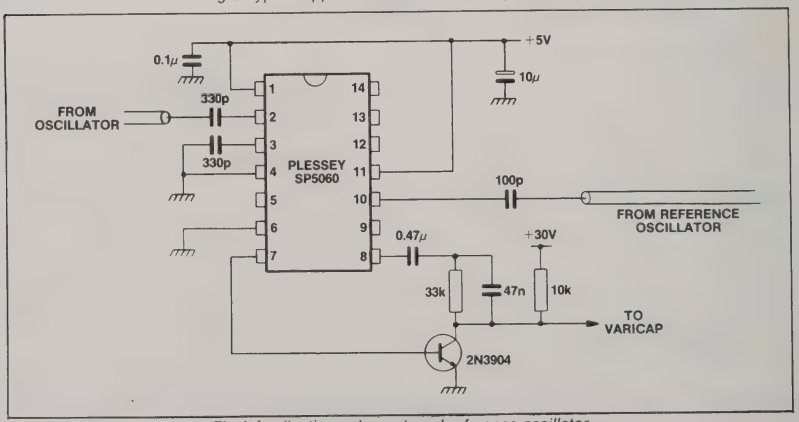

Fig.4 Application using external reference oscillator

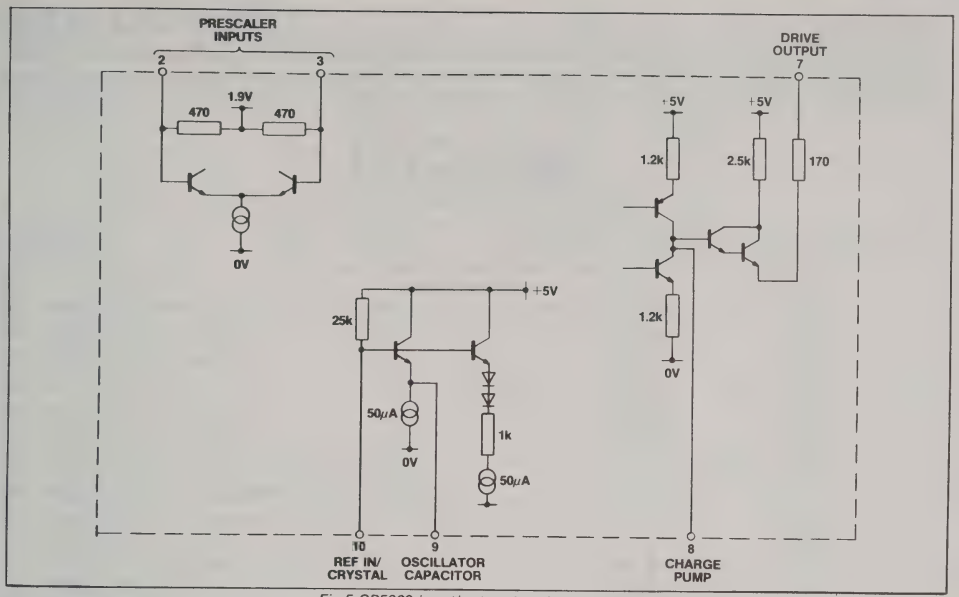

Fig.5 SP5060 input/output interface circuits

DESCRIPTION

The SP5060, when used with a voltage controlled oscillator, forms a complete phase locked loop frequency synthesiser.

The phase comparator reference frequency is obtained by dividing the reference frequency. This may be generated on chip, by means of a crystal, or from an external reference oscillator.

In order to achieve a high sensitivity at the voltage controlled oscillator pick off point, the divide-by-32 prescaler is preceded by a differential amplifier with inputs on pins 2 and 3. The output of the prescaler is divided by the fixed modulus divider, producing an output frequency which is phase locked to the reference frequency.

The divider stages are arranged to give a fixed ratio, between the synthesised frequency and the reference, of 256:1.

Any frequency within the range 300MHz to 1.8GHz may be achieved using the appropriate reference or crystal frequency.

A single external transistor, driven from the charge pump output, provides the output swing necessary for the oscillator varicap line.

To improve device stability the +5V and ground supplies to the chip are split and brought out to separate pins. It is therefore essential to connect all the supply pins for the device to operate correctly.

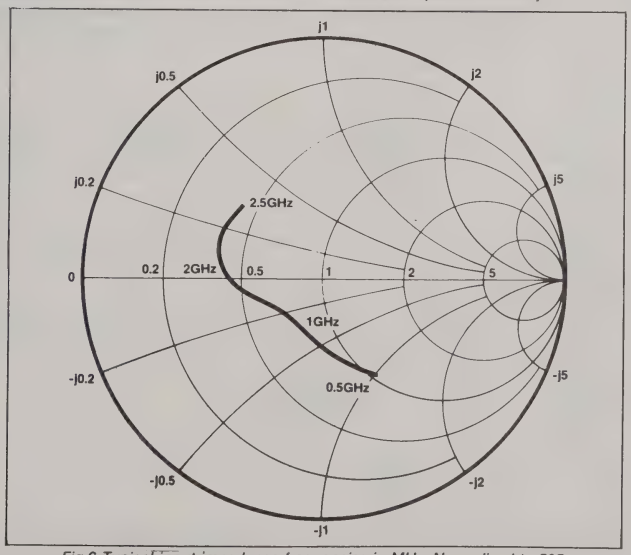

Fig.6 Typical input impedance frequencies in MHz. Normalised to 50Ω

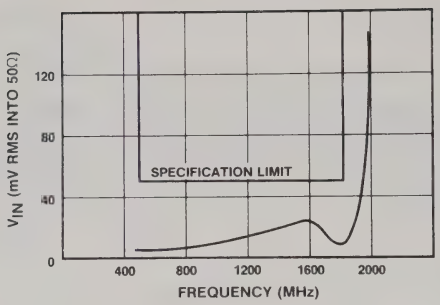

Fig.7 SP5060 typical input sensitivity

PLESSEY Semiconductors — ADVANCE INFORMATION — PIC SERIES

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PIC1650A

8 BIT MICROCOMPUTER

FEATURES

- User Programmable
- Intelligent Controller for Stand-Alone Applications
- 32 8-Bit RAM Registers
- 512 x 12-Bit Program ROM
- Arithmetic Logic Unit
- Real Time Clock Counter
- Self-contained Oscillator
- Access to RAM Registers Inherent in Instruction
- Wide Power Supply Operating Range (4.5V to 7.0V)
- Available in Two Temperature Ranges: 0° to 70°C and -40° to 85°C
- 4 Sets of 8 User Defined TTL-Compatible Input/ Output Lines
- 2 Level Stack

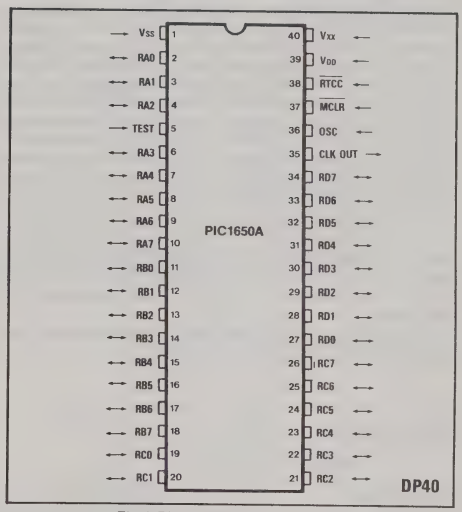


Fig.1 Pin connections - top view

The PIC1650A microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

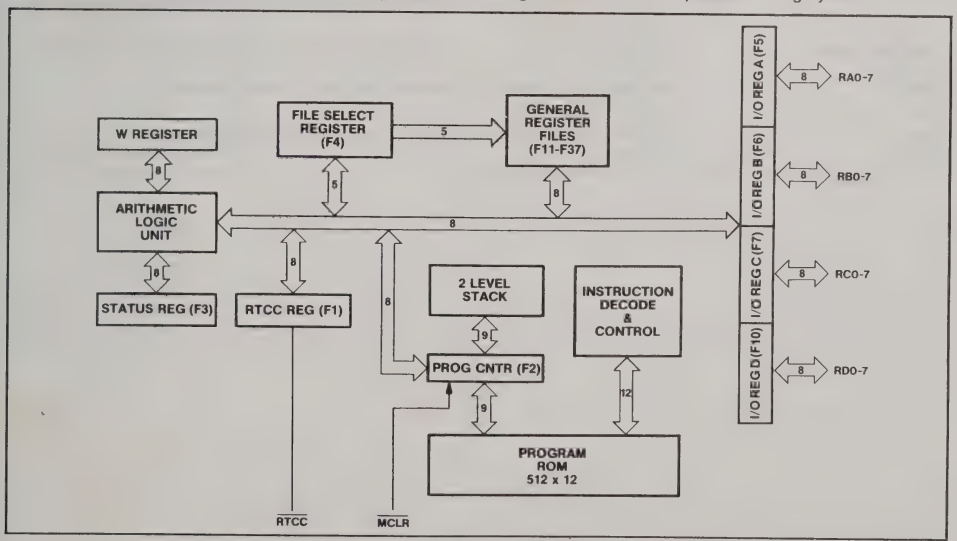


Fig. 2 PIC1650A block diagram

The PIC 1650A is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC 1664B. The PIC 1664B is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD 1000 Field Demo System is available containing a PIC 1664B with sockets for erasable CMOS PROMs. Finally, the PICES (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{MCLR}$ input on power up initializes the ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
OSC (input)	Oscillator input. This signal can be driven by an external oscillator if a precise frequency of operation is required or an external RC network can be used to set the frequency of operation of the internal clock generator. This is a Schmitt trigger input.
$\overline{RTCC}$ (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The RTCC register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input.
RA0-7, RB0-7, RC0-7, RD0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program.
$\overline{MCLR}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O register high. Should be held low at least 1ms past the time when the power supply is valid. This is a Schmitt trigger input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power. Used to enhance output current sinking capability.
V_{SS}	Ground

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$.
F2	Program Counter (PC).The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2).The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	I/O Register A (A0-A7)
F6	I/O Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10	I/O Register D (D0-D7)
F11-F37	General Purpose Registers

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f (FILE #)

For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1),f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇋f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations 0-377$_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting through a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data through an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

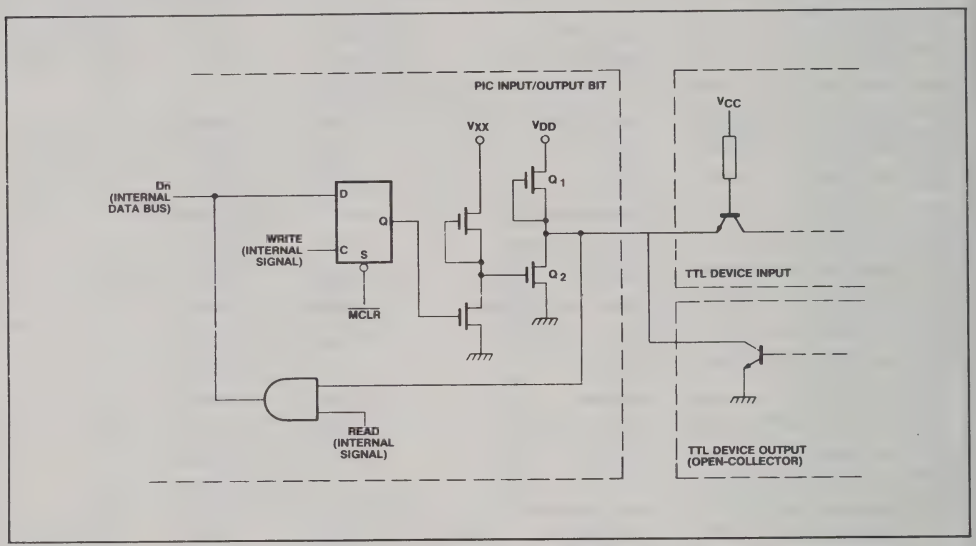


Fig.3 Typical interface - bidirectional I/O line

Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

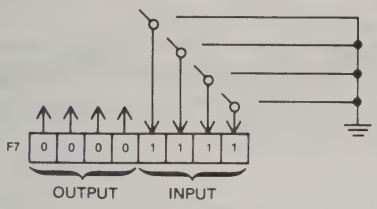
Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

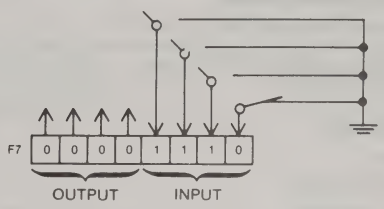


What is thought to be happening:
BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

Fig.4 Example 1



What could happen if an input were low:
BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

Fig.5 Example 2

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with Respect to V_{SS} ..... −0.3V to +12.0V
Power Dissipation 1000mW
Power Dissipated by any one I/O pin (Note 1) 60mW
Power Dissipated by all I/O pins (Note 1) 600mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{xx}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	55	mA	All I/O pins high
Output Buffer Supply Current	I_{xx}	—	1	5	mA	All I/O pins high (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC when driven externally)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 4)
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	I_{OL} = 1.6mA, V_{xx} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{xx} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{xx} = 8.0V
		—	—	1.20	V	I_{OL} = 10.0mA, V_{xx} = 8.0V
		—	—	2.0	V	I_{OL} = 20.0mA, V_{xx} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−10	—	+10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V

NOTES:
1. Power dissipation for I/O pins is calculated by
   $\Sigma (V_{CC} - V_{IL}) (|I_{IL}|) + \Sigma (V_{CC} - V_{OH}) (|I_{OH}|) + \Sigma (V_{OL}) (I_{OL})$.
   The term I/O refers to all interface pins; input, ouput or I/O.
2. V_{xx} supply drives only the I/O ports.
3. The maximum I_{xx} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.2MHz —1.0MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	t_{CY}	—	—	—	
High Pulse Width	t_{RTH}	½t_{CY}	—	—	—	
Low Pulse Width	t_{RTL}	½t_{CY}	—	—	—	(Note 2)
I/O Ports						
Data Input Setup Time	t_S	—	—	¼t_{CY}—125	ns	
Data Input Hold Time	t_H	0	—	—	ns	
Data Output Propagation Delay	t_{PD}	—	500	800	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High	R_{OSCH}	—	120	—	Ω	V_{OSC} = 5V } Applies to external
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	V_{OSC} = 0.4V } OSC drive only.

NOTES:

1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ input.

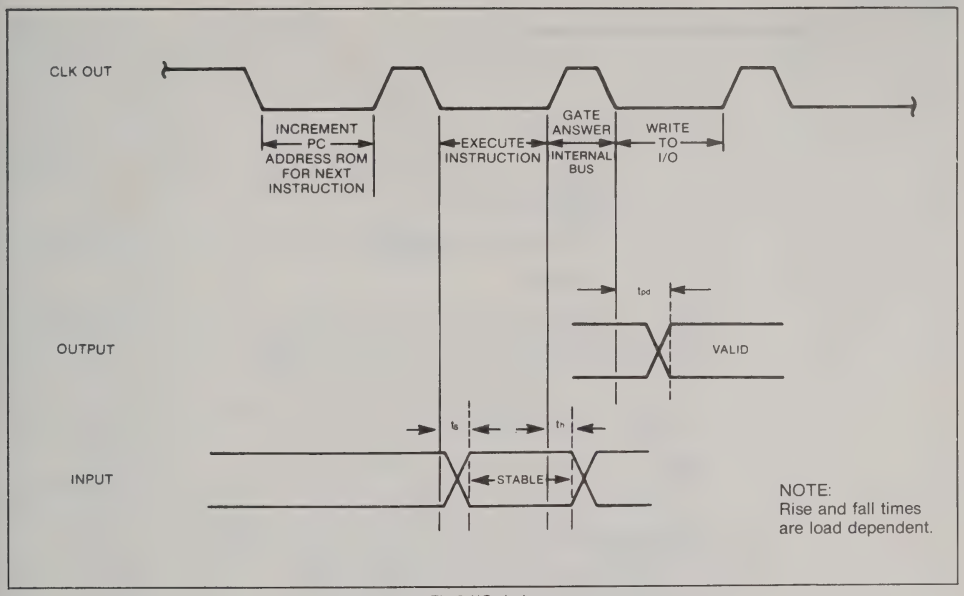


Fig.6 I/O timing

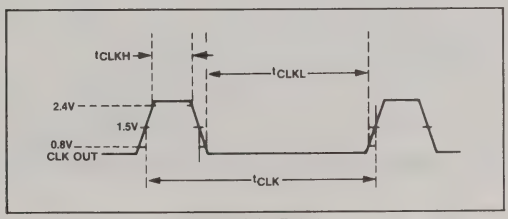


Fig.7 CLK OUT timing

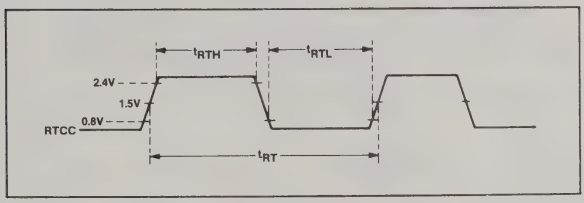


Fig.8 RTCC timing

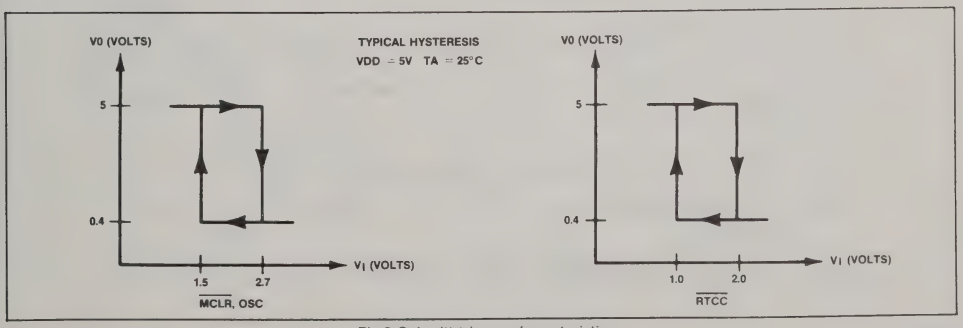


Fig.9 Schmitt trigger characteristics

PIC 1650A OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

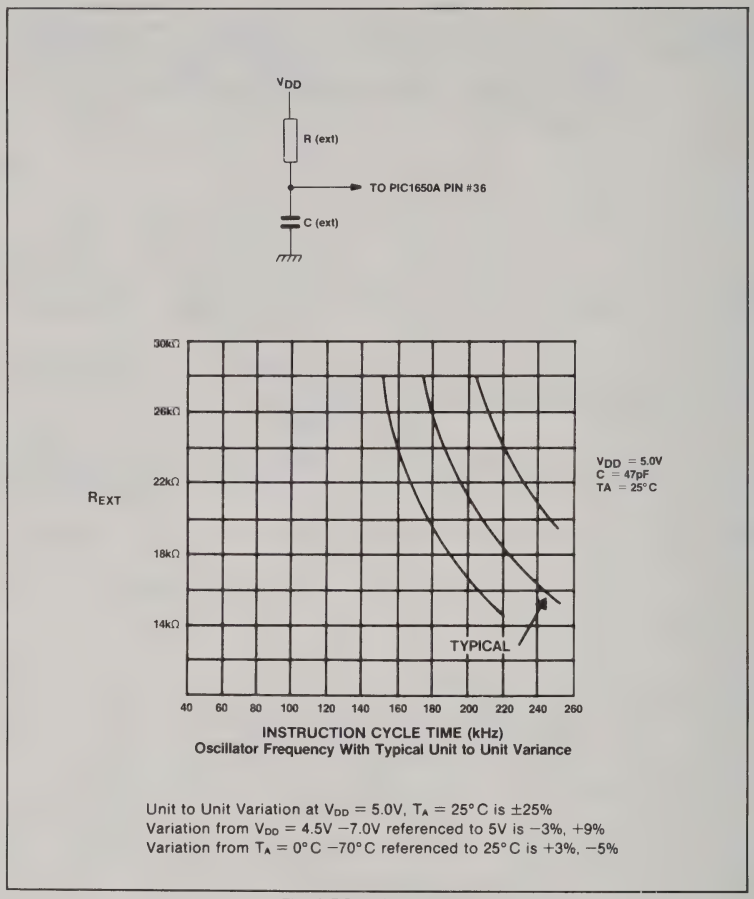

VDD
R (ext)
TO PIC1650A PIN #36
C (ext)
REXT
50kΩ
26kΩ
22kΩ
18kΩ
14kΩ
TYPICAL
VDD = 5.0V
C = 47pF
TA = 25°C
40 60 80 100 120 140 160 180 200 220 240 260
INSTRUCTION CYCLE TIME (kHz)
Oscillator Frequency With Typical Unit to Unit Variance
Unit to Unit Variation at VDD = 5.0V, TA = 25°C is ±25%
Variation from VDD = 4.5V −7.0V referenced to 5V is −3%, +9%
Variation from TA = 0°C −70°C referenced to 25°C is +3%, −5%

Fig.10 RC option operation

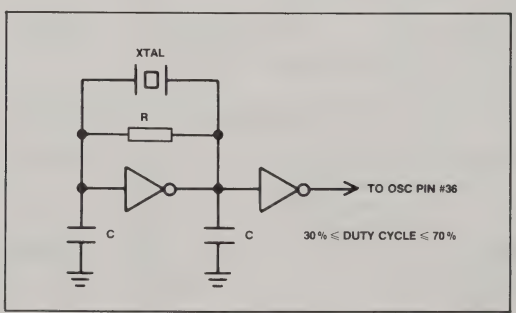


Fig.11 Buffered crystal input operation

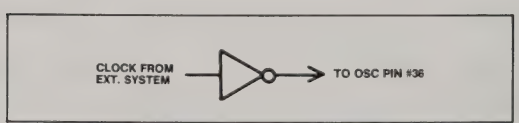
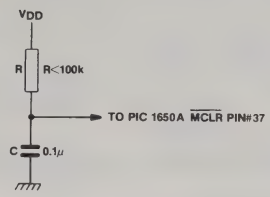
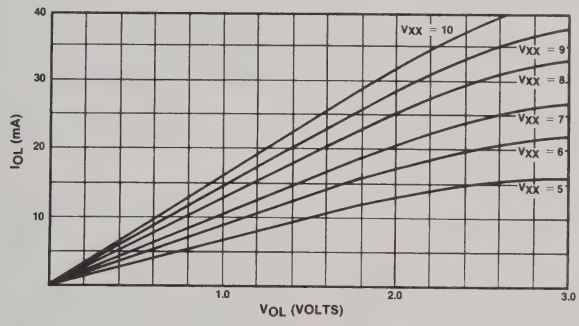


Fig.12 External clock input operation



Master Clear requires > 1.0ms delay before activation after power is applied to the V_{DD} pin. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

Fig.13 Master clear



The Output Sink Current is dependent on the V_{XX} supply and the output load. This chart shows the typical curves used to express the output drive capability.

Fig.14 Output sink current graph

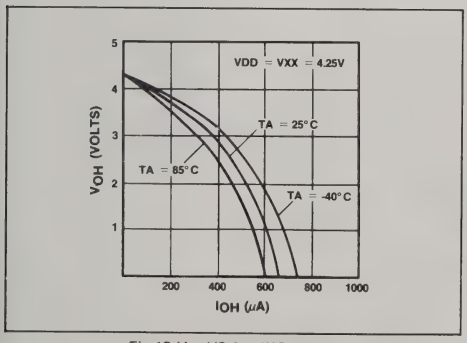


Fig.15 V_{OH} VS I_{OH} (I/O ports)

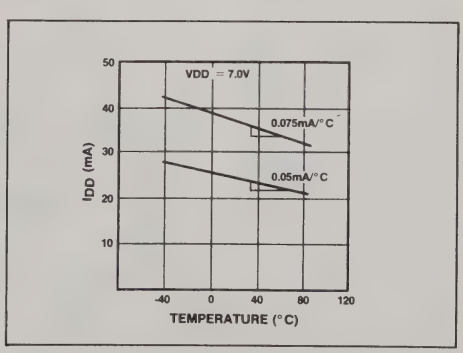


Fig.16 Power supply current vs temperature

PIC1650A EMULATION CAUTIONS

When emulating a PIC1650A using a PICES development system certain precautions should be taken.

A. Be sure that the PICES Module being used is programmed for the PIC1650A mode. (Refer to PICES Manual). The PIC1664B contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{\text{MCLR}}$ to force all I/O registers high.
2. The OSC 1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 40 pin socket for the module plug.

E. Make sure that during an actual application that the $\overline{\text{MCLR}}$ input swings from a low to high level a minimum of 1msec after the supply voltage is applied.

F. If an external oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC1650A.

G. The cable length and internal variations may cause some parameter values to differ between the PICES module and a production PIC1650A.

PLESSEY Semiconductors

ADVANCE INFORMATION

PIC SERIES

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

PIC1655A

8 BIT MICROCOMPUTER

FEATURES

- User Programmable
- Intelligent Controller for Stand-Alone Applications
- 32 8-Bit RAM Registers
- 512 x 12-Bit Program ROM
- Arithmetic Logic Unit
- Real Time Clock Counter
- Self-contained Oscillator
- Access to RAM Registers Inherent in Instruction
- Wide Power Supply Operating Range (4.5V to 7.0V)
- Available in Two Temperature Ranges: 0°C to 70°C and -40°C to 85°C
- 4 Inputs, 8 Outputs, 8 Bidirectional I/O Lines
- 2 Level Stack

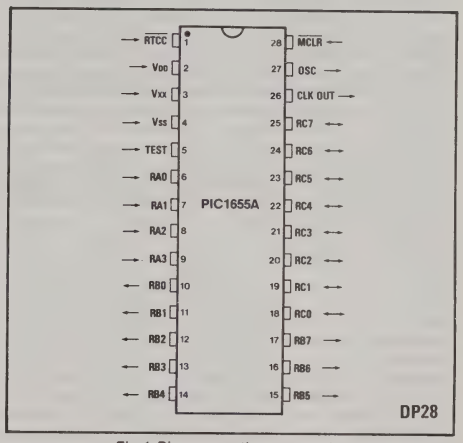


Fig.1 Pin connections - top view

The PIC1655A microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios,

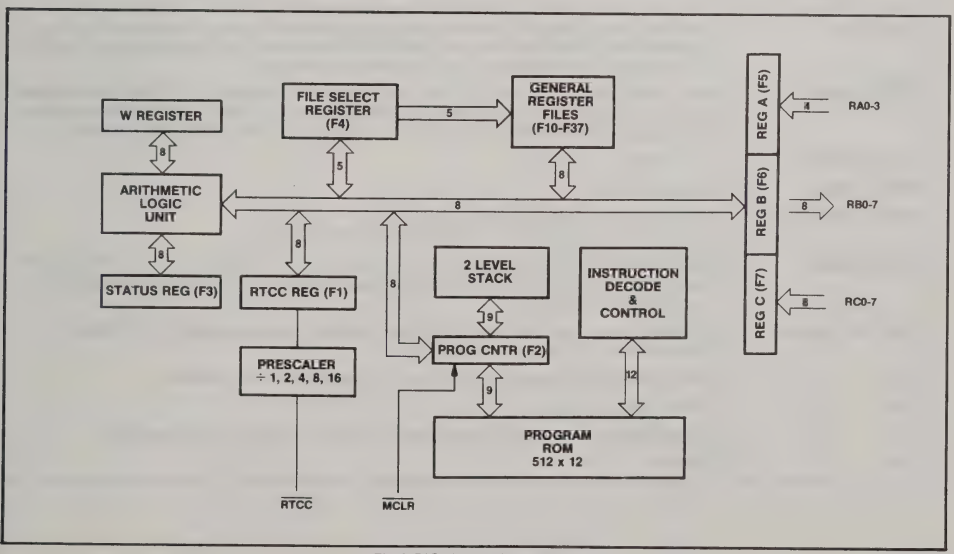


Fig.2 PIC1655A block diagram

television, consumer appliances, Industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1655A is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1664B. The PIC1664B is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD 1000 Field Demo System is available containing a PIC1664B with sockets for erasable CMOS PROMs. Finally, the PICES (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or opertion as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the MCLR input on power up initializes the ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
OSC (input)	Oscillator input: This signal can be driven by an external oscillator if a precise frequency of operation is required or an external RC network can be used to set the frequency of operation of the internal clock generator. This is a Schmitt trigger input.
$\overline{\text{RTCC}}$ (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The Real Time Clock Counter Register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input.
RA0-3 (input)	4 input lines
RB0-7 (output)	8 output lines
RC0-7 (input/output)	8 user programmable input/output lines All inputs and outputs are under direct control of the program.
$\overline{\text{MCLR}}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O register high. Should be held low at least 1ms past the time when the power supply is valid. This is a Schmitt trigger input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power supply. Used to enhance output current sinking capability.
V_{SS}	Ground

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3) (A4-A7 defined as zeroes).
F6	Output Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10-F37	General Purpose Registers

BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f (FILE #)

For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇆f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting through a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data through an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

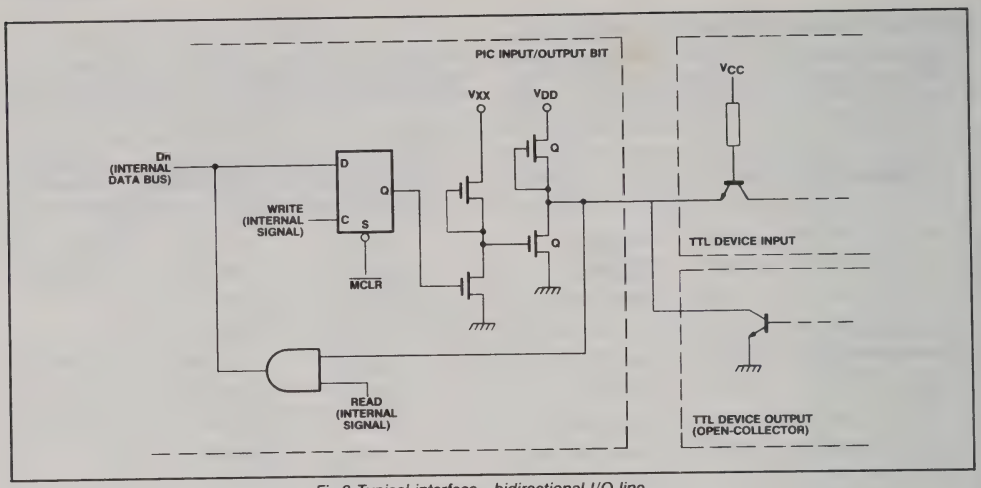


Fig.3 Typical interface - bidirectional I/O line

Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Input Only Port: (Port RA)

The input only port of the PIC1655A consists of the four LSB's of F5 (port RA). An internal pull-up device is provided so that external pull-ups on open collector logic are unnecessary. The four MSB's of this port are always read as zeros. Output operatins to F5 are not defined. Note that the BTFSC and BTFSS instructions are input only operations and so can be used with F5.

Output Only Port: (Port RB)

The output only port of the PIC1655A consists of F6 (port RB). This port contains no input circuitry and is therefore not capable of instructions requiring an input followed by an output operation. The only instructions which can validly use F6 are MOVWF and CLRF.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction whic causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

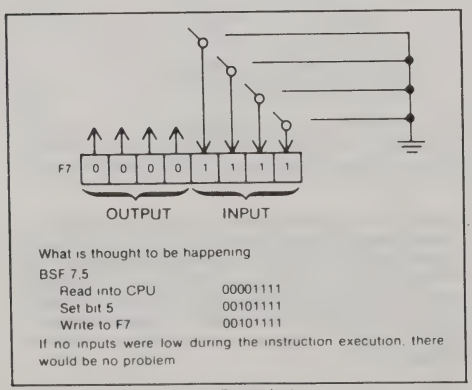

F7
0 0 0 0 1 1 1 1
OUTPUT
INPUT
What is thought to be happening
BSF 7,5
Read into CPU 00001111
Set bit 5 00101111
Write to F7 00101111
If no inputs were low during the instruction execution, there would be no problem

Fig.4 Example 1

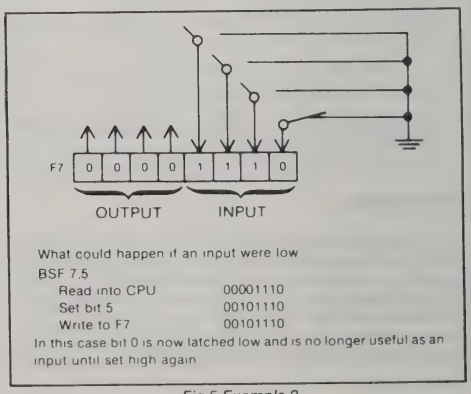

F7
0 0 0 0 1 1 1 0
OUTPUT
INPUT
What could happen if an input were low
BSF 7,5
Read into CPU 00001110
Set bit 5 00101110
Write to F7 00101110
In this case bit 0 is now latched low and is no longer useful as an input until set high again

Fig.5 Example 2

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with Respect to Vss ..... −0.3V to +12.0V
Power Dissipation 1000mW
Power Dissipated by any one I/O pin (Note 1) 60mW
Power Dissipated by all I/O pins (Note 1) 300mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{xx}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	50	mA	All I/O pins high
Output Buffer Supply Current	I_{xx}	—	1	5	mA	All I/O pins high (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC when driven externally)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 4)
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	I_{OL} = 1.6mA, V_{xx} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{xx} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{xx} = 8.0V
		—	—	1.20	V	I_{OL} = 10.0mA, V_{xx} = 8.0V
		—	—	2.0	V	I_{OL} = 20.0mA, V_{xx} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−10	—	+10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V

NOTES:

1. Power dissipation for I/O pins is calculated by
   $\Sigma (V_{CC} - V_{IL}) (|I_{IL}|) + \Sigma (V_{CC} - V_{OH}) (|I_{OH}|) + \Sigma (V_{OL}) (I_{OL})$.
   The term I/O refers to all interface pins; input, ouput or I/O.
2. V_{xx} supply drives only the I/O ports.
3. The maximum I_{xx} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature $T_A = 0°C$ to $+70°C$

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.2MHz −1.0MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	t_{CY}	—	—	—	
High Pulse Width	t_{RTH}	$\frac{1}{2}t_{CY}$	—	—	—	
Low Pulse Width	t_{RTL}	$\frac{1}{2}t_{CY}$	—	—	—	(Note 2)
I/O Ports						
Data Input Setup Time	t_S	—	—	$\frac{1}{4}t_{CY}-125$	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	800	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High	R_{OSCH}	—	120	—	Ω	$V_{OSC} = 5V$ } Applies to external
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	$V_{OSC} = 0.4V$ } OSC drive only.

NOTES:

1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ input.

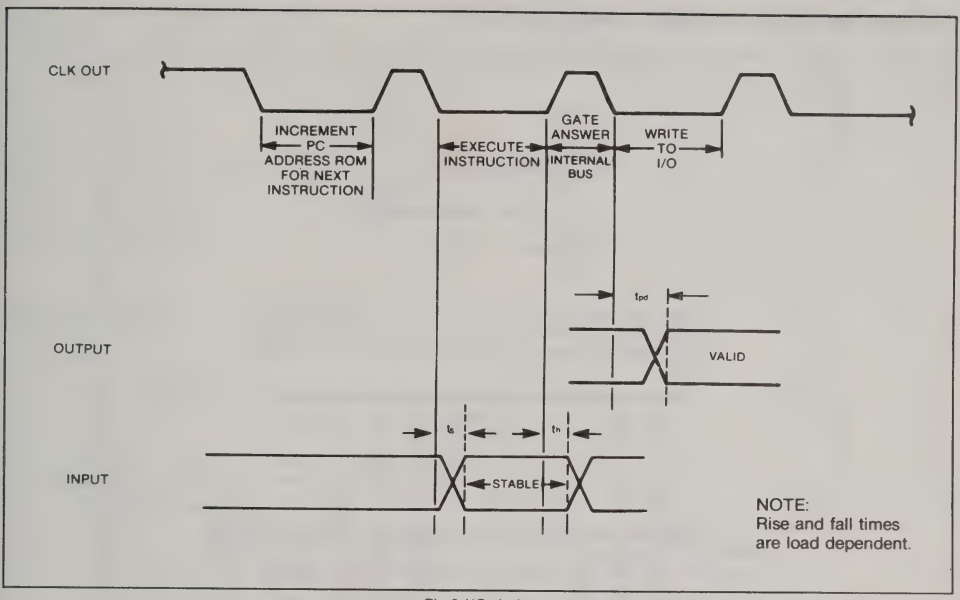


Fig.6 I/O timing

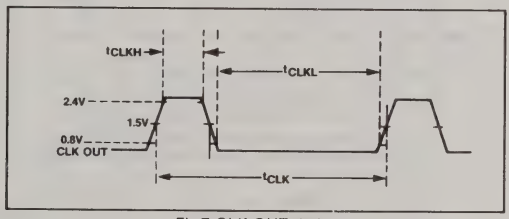


Fig.7 CLK OUT timing

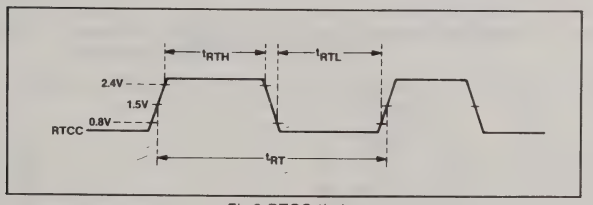


Fig.8 RTCC timing

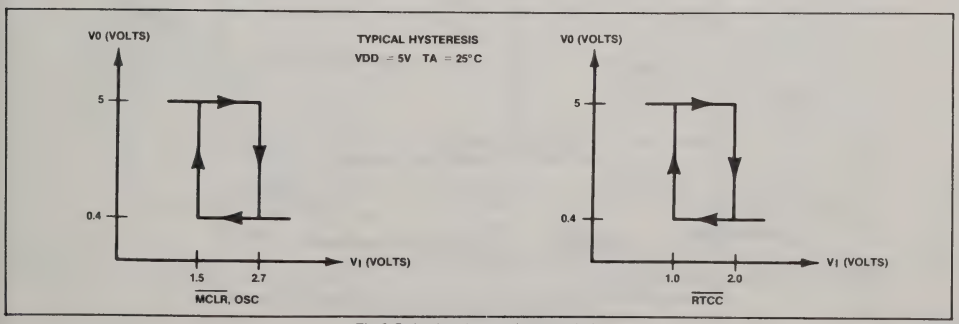


Fig.9 Schmitt trigger characteristics

PIC1655A OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

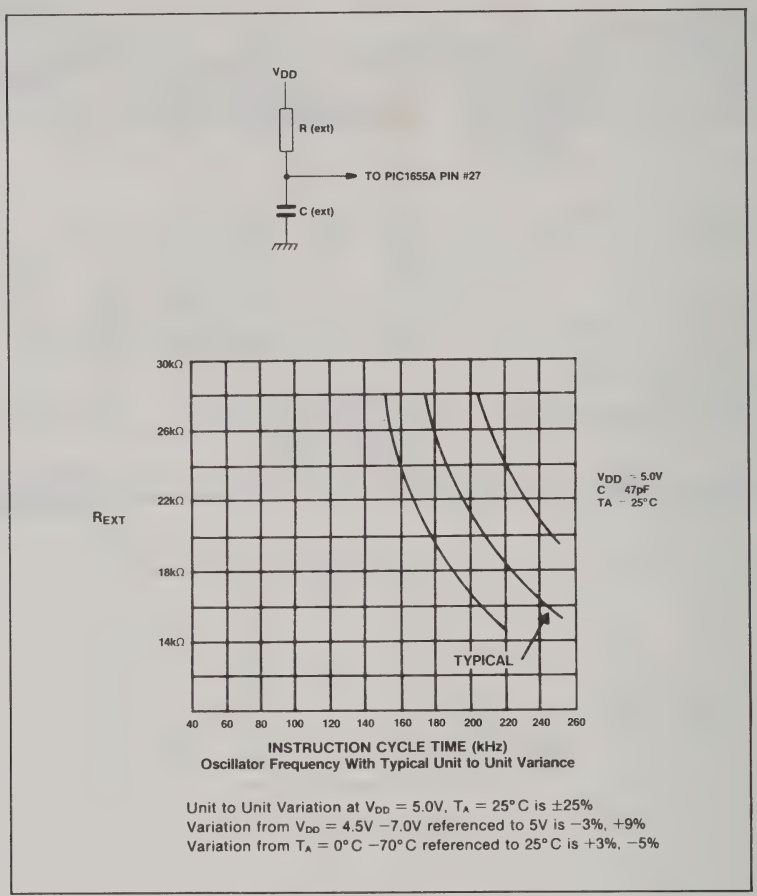

VDD
R (ext)
TO PIC1655A PIN #27
C (ext)
REXT
30kΩ
26kΩ
22kΩ
18kΩ
14kΩ
VDD = 5.0V
C = 47pF
TA = 25°C
TYPICAL
40 60 80 100 120 140 160 180 200 220 240 260
INSTRUCTION CYCLE TIME (kHz)
Oscillator Frequency With Typical Unit to Unit Variance
Unit to Unit Variation at VDD = 5.0V, TA = 25°C is ±25%
Variation from VDD = 4.5V −7.0V referenced to 5V is −3%, +9%
Variation from TA = 0°C −70°C referenced to 25°C is +3%, −5%

Fig.10 RC option operation

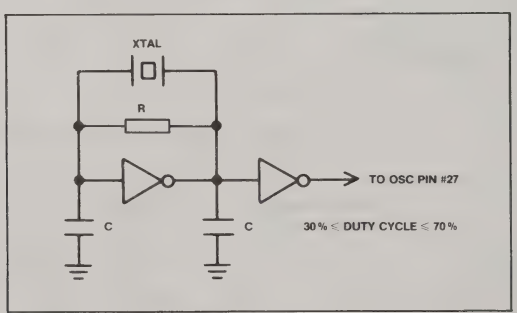


Fig.11 Buffered crystal input operation

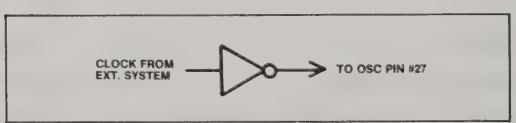
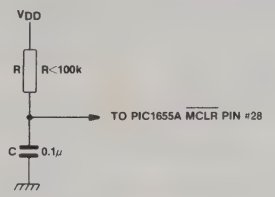
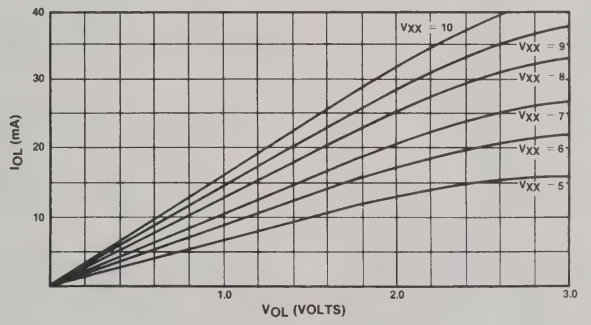


Fig.12 External clock input operation



Master Clear requires > 1.0ms delay before activation after power is applied to the VDD pin. To achieve this, an external RC configuration as shown can be used (assuming VDD is applied as a step function).

Fig.13 Master clear



IOL vs. VOL TYP @ 25°C

The Output Sink Current is dependent on the VXX supply and the output load. This chart shows the typical curves used to express the output drive capability.

Fig.14 Output sink current graph

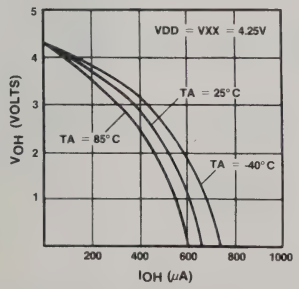


Fig.15 VOH vs. IOH (I/O ports)

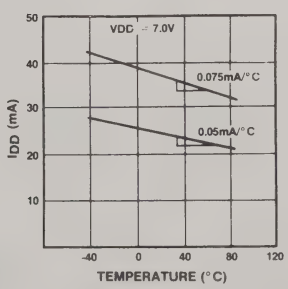


Fig.16 Power supply current vs. temperature

PIC1655A EMULATION CAUTIONS

When emulating a PIC1655A using a PICES development system certain precautions should be taken.

A. Be sure that the PICES Module being used is programmed for the PIC1655A mode. (Refer to PICES Manual). The PIC1664B contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{MCLR}$ to force all I/O registers high.
2. The OSC 1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 40 pin socket for the module plug.

E. Make sure that during an actual application that the $\overline{MCLR}$ input swings from a low to high level a minimum of 1msec after the supply voltage is applied.

F. If an external oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC1655A.

G. The cable length and internal variations may cause some parameter values to differ between the PICES module and a production PIC1655A.

PLESSEY Semiconductors — ADVANCE INFORMATION — PIC SERIES

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

PIC1655XT

8 BIT MICROCOMPUTER

FEATURES

- User Programmable
- Intelligent Controller for Stand-Alone Applications
- 32 8-Bit RAM Registers
- 512 x 12-Bit Program ROM
- Arithmetic Logic Unit
- Real Time Clock Counter
- Self-contained Crystal Oscillator
- Access to RAM Registers Inherent in Instruction
- Wide Power Supply Operating Range (4.5V to 7.0V)
- Available in Two Temperature Ranges: 0° to 70°C and -40° to 85°C
- 4 Inputs, 8 Outputs, 8 Bidirectional I/O Lines
- 2 Level Stack
- Mask Programmable Prescaler for RTCC
- Mask Programmable Open Drain Option on all I/O Lines

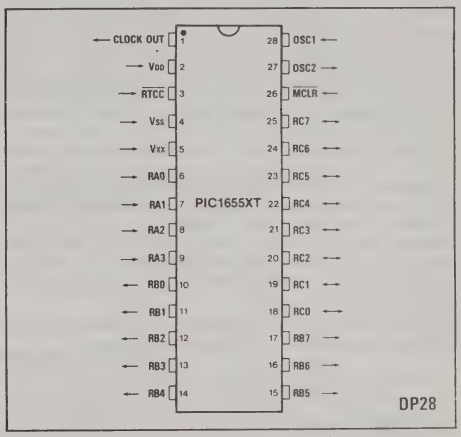


Fig.1 Pin connections - top view

The PIC1655XT microcomputer is a MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial

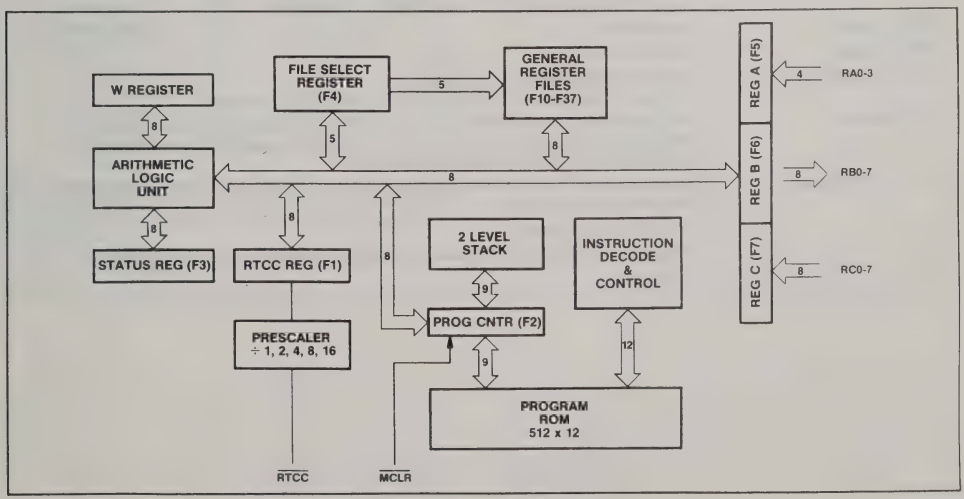


Fig.2 PIC1655XT block diagram

timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1655XT is fabricated with N-channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for opertion, and an on-chip oscillator provides the operating clock with an external crystal, ceramic resonator or LC network to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC 1664B. The PIC 1664B is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD 1000 Field Demo System is available containing a PIC 1664B with sockets for erasable CMOS PROMs. Finally, the PICES (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{\text{MCLR}}$ input on power up initializes the ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
OSC1 (input), OSC2 (output)	Oscillator pins. The oscillator frequency can be set by a crystal, ceramic resonator, external LC network or driven externally. The oscillator frequency is sixteen times the instruction frequency.
RTCC (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The Real Time Clock Counter, Register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input except when a prescaler division ratio of 2,4,8 or 16 is selected in which case the input is TTL compatible.
RA0-3 (input)	4 input lines
RB0-7 (output)	8 output lines
RC0-7 (input/output)	8 user programmable input/output lines All inputs and outputs are under direct control of the program.
MCLR (input)	Master Clear. Used to initialize the internal ROM program to address 777, and latch all I/O registers high. Should be held low at least 1ms past the time when power supply is valid. This is a Schmitt trigger input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power supply. Used to enhance output current sinking capability.
V_{SS}	Ground

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$.
F2	Program Counter (PC).The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2).The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3) (A4-A7 defined as zeroes).
F6	Output Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10-F37	General Purpose Registers

The PIC1655XT has the same basic architecture as the PIC1655A with the additional enhancements described below.

Real Time Clock Counter

The Real Time Clock Counter can be read from and written to under software control. In addition, it can be used to count external events via the RTCC input. A prescaler counter between the RTCC input and the Real Time Clock Counter can be mask programmed to enable the RTCC register to increment every 1,2,4,8, or 16 negative edges of the RTCC input pin.

This allows the maximum frequency of the RTCC input to be (assume an instruction cycle time of 4μs):

Prescaler Division Ratio	Maximum Input Frequency
1	0.238MHz
2	0.476MHz
4	0.952MHz
8	1.904MHz
16	3.808MHz

NOTE

The Schmitt trigger input is valid only when a division ratio of 1 is selected. Otherwise, the input is a normal TTL compatible input.

Self-Contained Oscillator

When a crystal, ceramic resonator or LC network is connected between the OSC1 and OSC2 pins, the self-contained oscillator will generate a frequency determined by the external components thus allowing an accurate timing reference, a crystal, to be used for time base control with a minimum of external parts.

The output of this oscillator is divided down by 16 to give the instruction cycle time of the microcomputer, thus with a 4MHz crystal the instruction cycle time is 4μs.

BASIC INSTRUCTION SET SUMMARY

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f (FILE #)

For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)≒f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting through a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data through an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

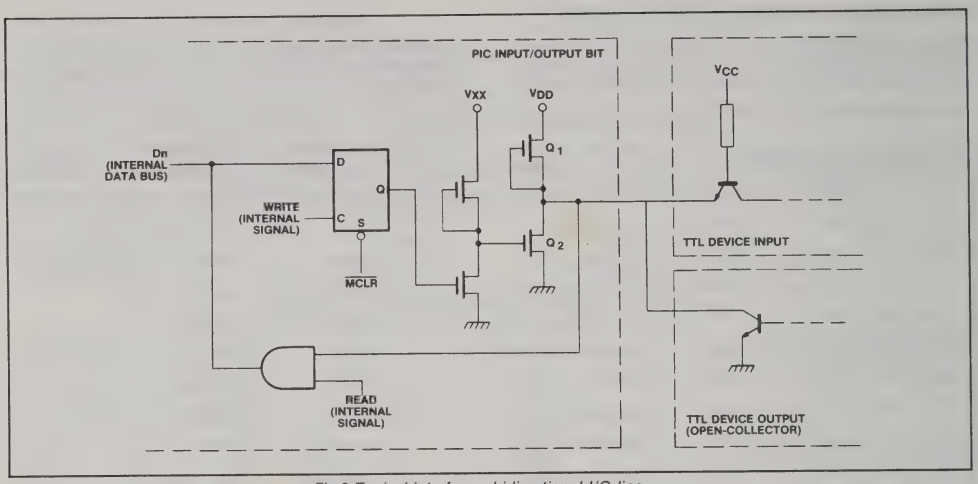


Fig.3 Typical interface - bidirectional I/O line

Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an inut instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Input Only Port: (Port RA)

The input only port of the PIC1655XT consists of the four LSB's of F5 (port RA). An internal pull-up device is provided so that external pull-ups on open collector logic are unnecessary. The four MSB's of this port are always read as zeroes. Output operations to F5 are not defined. Note that the BTFSC and BTFSS instructions are input only operations and so can be used with F5.

Output Only Port: (Port RB)

The output only port of the PIC1655XT consists of F6 (port RB). This port contains no input circuitry and is therefore not capable of instructions requiring an input followed by an output operation. The only instructions which can validly use F6 are MOVWF and CLRF.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than t_{cy} (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

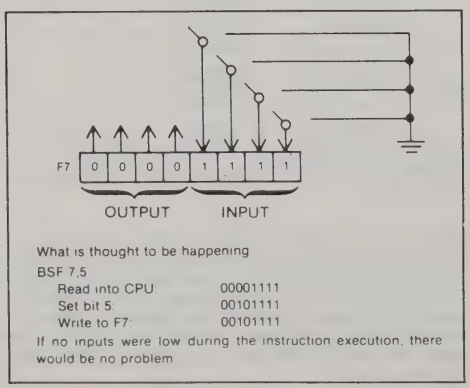

F7
0 0 0 0 1 1 1 1
OUTPUT
INPUT
What is thought to be happening
BSF 7,5
Read into CPU: 00001111
Set bit 5: 00101111
Write to F7: 00101111
If no inputs were low during the instruction execution, there would be no problem

Fig.4 Example 1

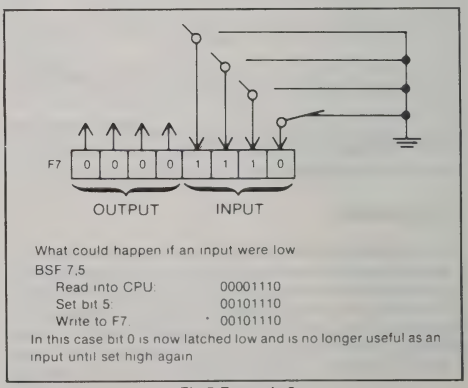

F7
0 0 0 0 1 1 1 0
OUTPUT
INPUT
What could happen if an input were low
BSF 7,5
Read into CPU: 00001110
Set bit 5: 00101110
Write to F7: 00101110
In this case bit 0 is now latched low and is no longer useful as an input until set high again

Fig.5 Example 2

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with Respect to V_{SS} ..... −0.3V to +12.0V
Power Dissipation 1000mW
Power Dissipated by any one I/O pin (Note 1) 60mW
Power Dissipated by all I/O pins (Note 1) 300mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{xx}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	50	mA	All I/O pins high
Output Buffer Supply Current	I_{xx}	—	1	5	mA	All I/O pins high (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC when driven externally)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 4)
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	I_{OL} = 1.6mA, V_{xx} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{xx} = 4.5V
		—	—	0.40	V	I_{OL} = 5.0mA, V_{xx} = 8.0V
		—	—	1.20	V	I_{OL} = 10.0mA, V_{xx} = 8.0V
		—	—	2.0	V	I_{OL} = 20.0mA, V_{xx} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−10	—	+10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V

NOTES:

1. Power dissipation for I/O pins is calculated by
   $\Sigma (V_{CC} - V_{IL}) (|I_{IL}|) + \Sigma (V_{CC} - V_{OH}) (|I_{OH}|) + \Sigma (V_{OL}) (I_{OL})$.
   The term I/O refers to all interface pins; input, ouput or I/O.
2. V_{xx} supply drives only the I/O ports.
3. The maximum I_{xx} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 175mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.8MHz-4MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	t_{CY}	—	—	—	
High Pulse Width	t_{RTH}	½t_{CY}	—	—	—	
Low Pulse Width	t_{RTL}	½t_{CY}	—	—	—	(Note 2)
I/O Ports						
Data Input Setup Time	t_S	—	—	¼t_{CY}−125	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	800	ns	Capacitive load = 50pF

NOTES
1. Instruction cycle period (t_{CY}) equals sixteen times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ input.
3. If an $\overline{RTCC}$ prescaler division ratio of 2,4,8 or 16 is selected, the maximum rise and fall times of the signal input to the $\overline{RTCC}$ pin is 200nsecs and its duty cycle must be between 40% and 60%.
4. The maximum frequency which may be input to the $\overline{RTCC}$ pin for a division ratio of 1 is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$

For example:

$$\text{if } t_{CY} = 4\mu s,\ f_{(max)} = \frac{1}{4.2\mu s} = 238kHz$$

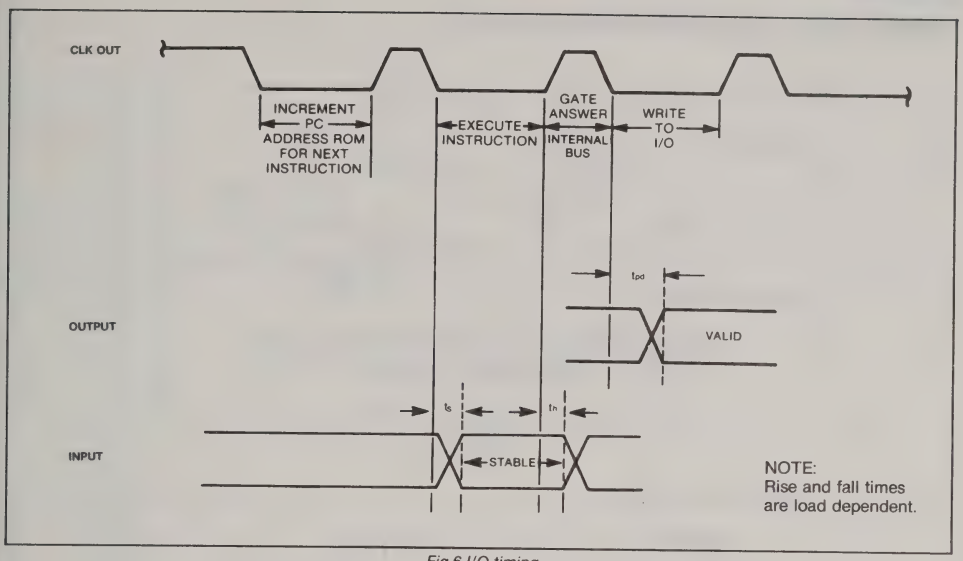


Fig.6 I/O timing

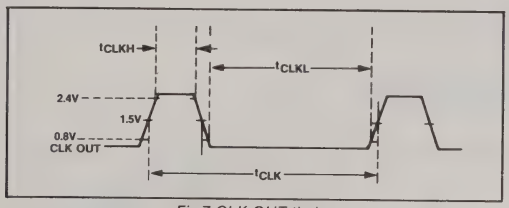


Fig.7 CLK OUT timing

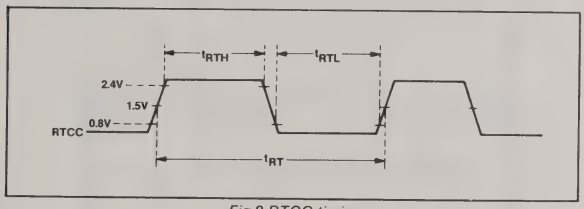


Fig.8 RTCC timing

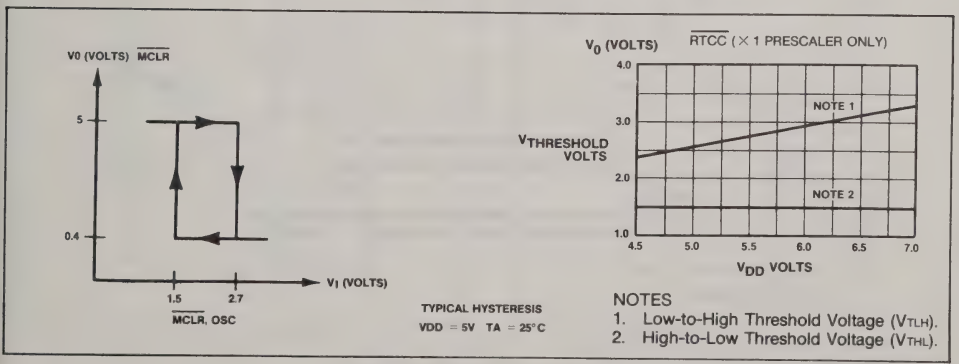


Fig.9 Schmitt trigger characteristics

PIC1655XT OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

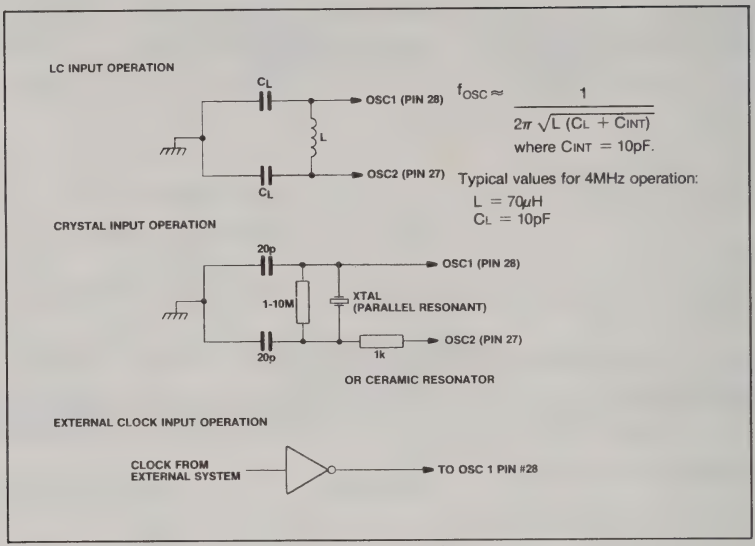


Fig.10 Oscillator options

POWER DISSIPATION DERATING GRAPH

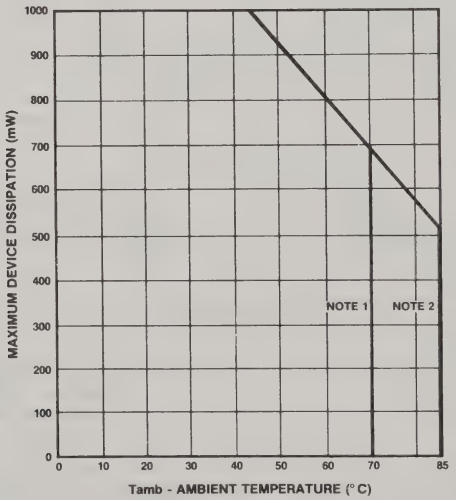
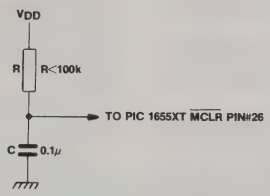


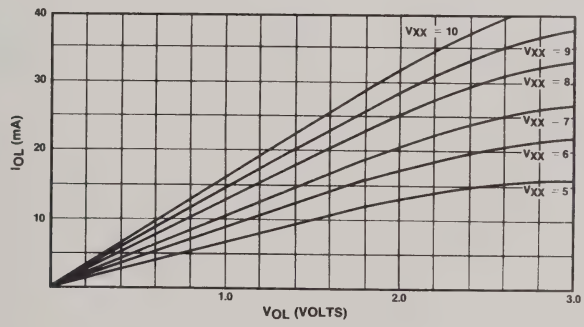
Fig.11 Power dissipation derating graph

NOTES:
1. 70° C is the maximum operating temperature for standard parts.
2. 85° C is the maximum operating temperature for "I" suffix parts.



Master Clear requires > 1.0ms delay before activation after power is applied to the V_{DD} pin. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

Fig.12 Master clear



The Output Sink Current is dependent on the V_{XX} supply and the output load. This chart shows the typical curves used to express the output drive capability.

Fig.13 Output sink current graph

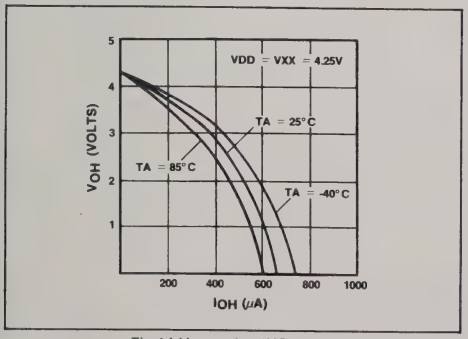


Fig.14 V_{OH} vs. I_{OH} (I/O ports)

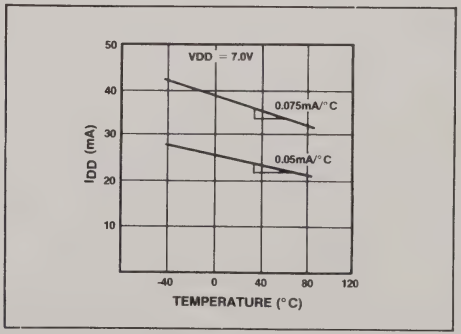


Fig.15 Power supply current vs. temperature

PIC1655XT EMULATION CAUTIONS

When emulating a PIC1655XT using a PICES- II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1655XT mode. (Refer to PICES II Manual). The PIC1664 contained within the module should have the MODE pin #22 set to a high state.
   1. This causes the MCLR to force all I/O registers high.
   2. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
   3. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

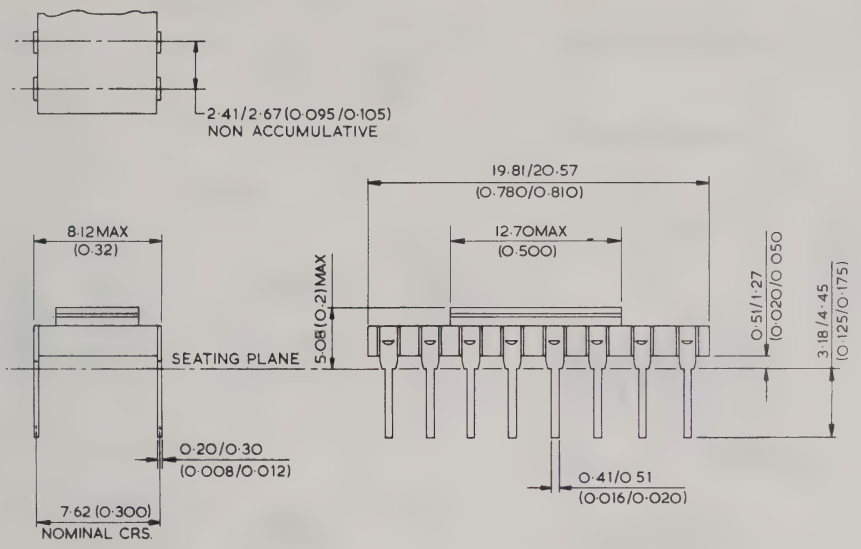
D. Be sure to use the 28 pin socket for the module pin.

E. Make sure that during an actual application the MCLR input swings from a low to high level a minimum of 10msec after the supply voltage is applied to allow for the crystal to start up.

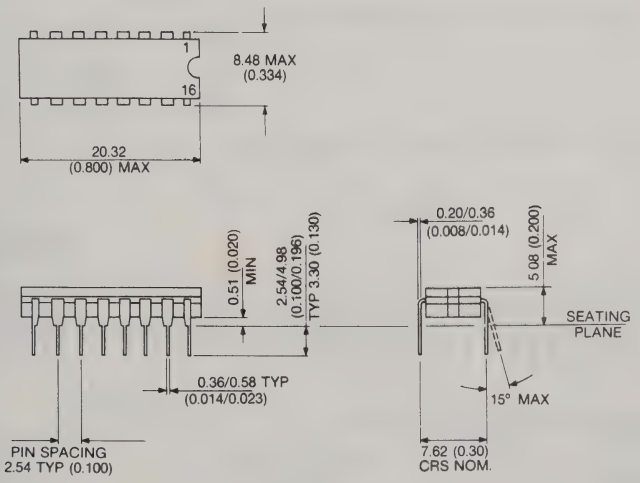
F. The cable length and internal variations may cause some parameter values to differ between PICES II Module and a production PIC1655XT.

G. The emulator PFD board or PICES II Module offers only 'internal' oscillator operation (i.e. the crystal is on the PFD or Module Board) as the long cable might cause unreliable crystal operation.

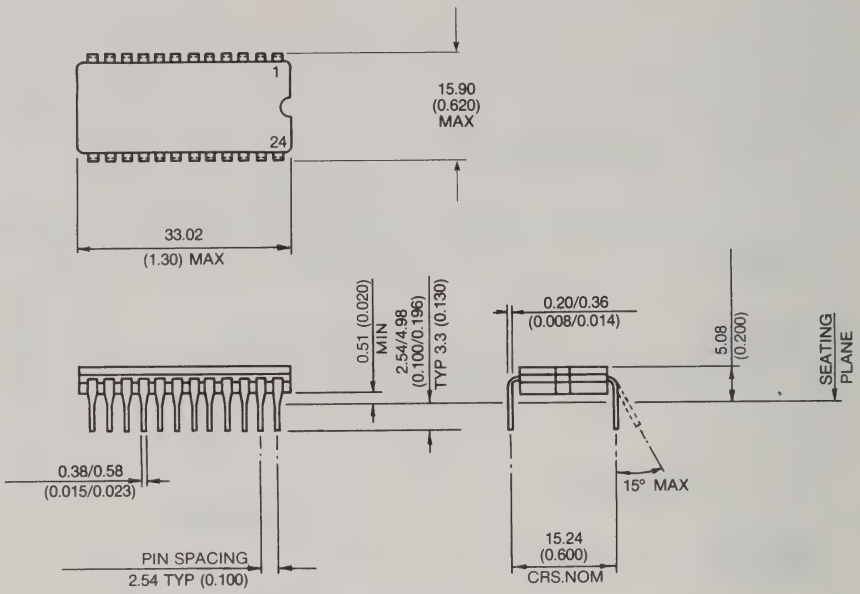
Package Outlines



16 LEAD DILMON **DC16**

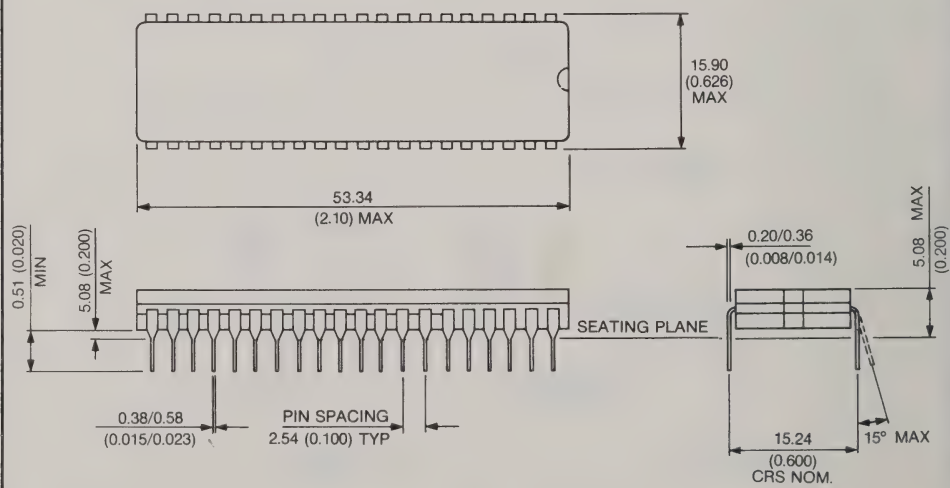


16 LEAD CERAMIC DIL
CERDIP - DG16 **DG16**



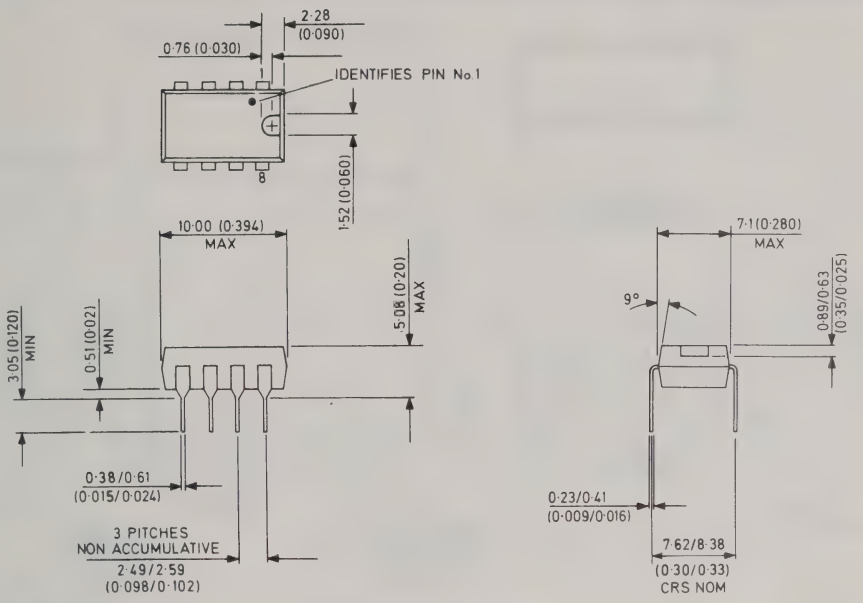
24 LEAD CERAMIC DIL
CERDIP - DG24

DG24

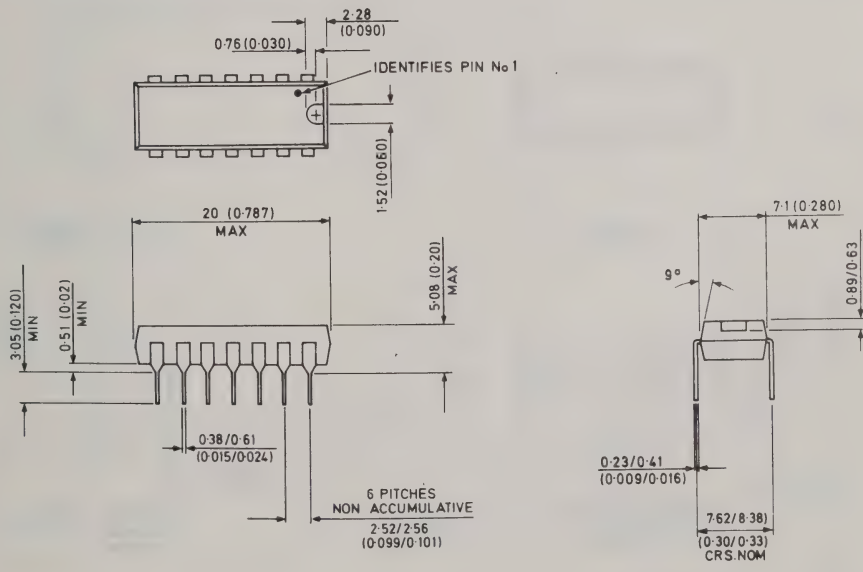


40 LEAD CERAMIC DIL
CERDIP - DG40

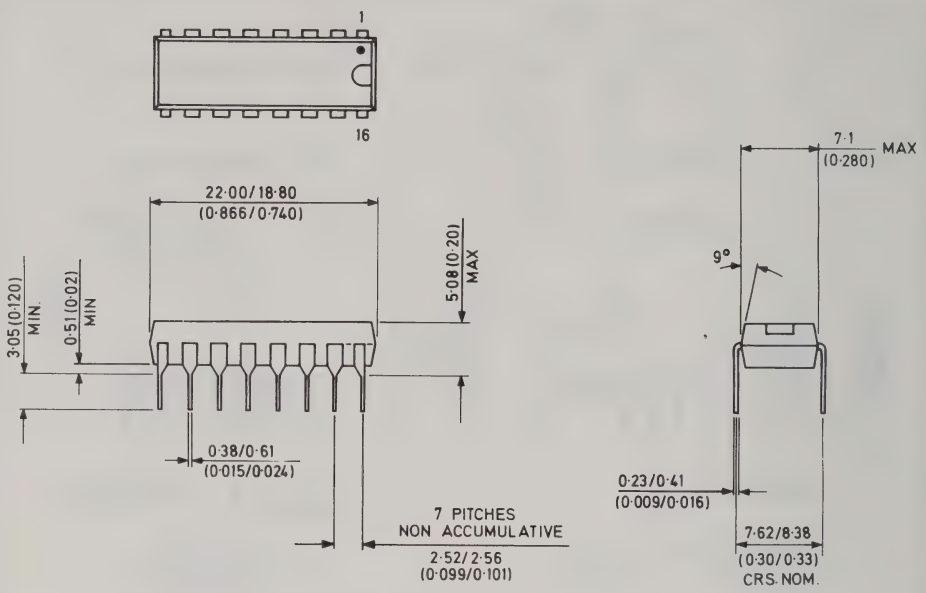
DG40



8 LEAD PLASTIC DIL **DP8**



14 LEAD PLASTIC DIL **DP14**



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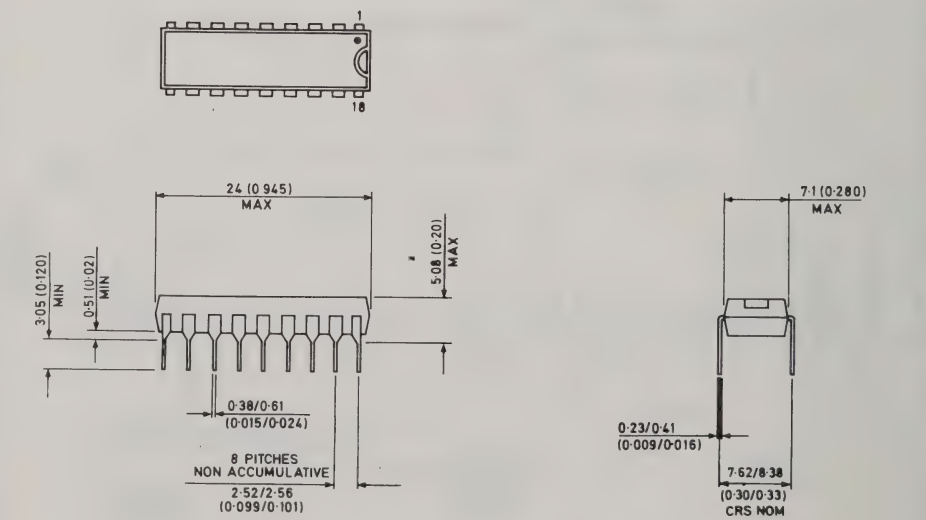

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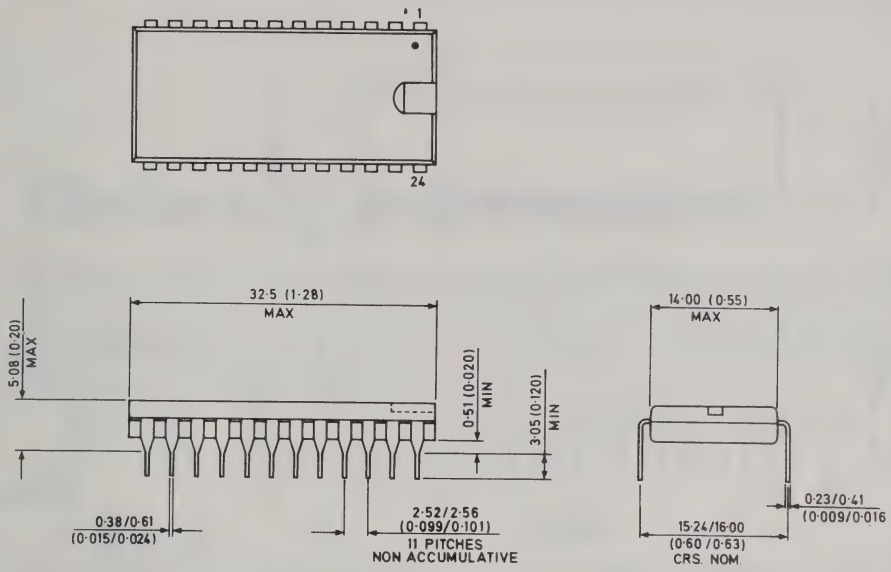

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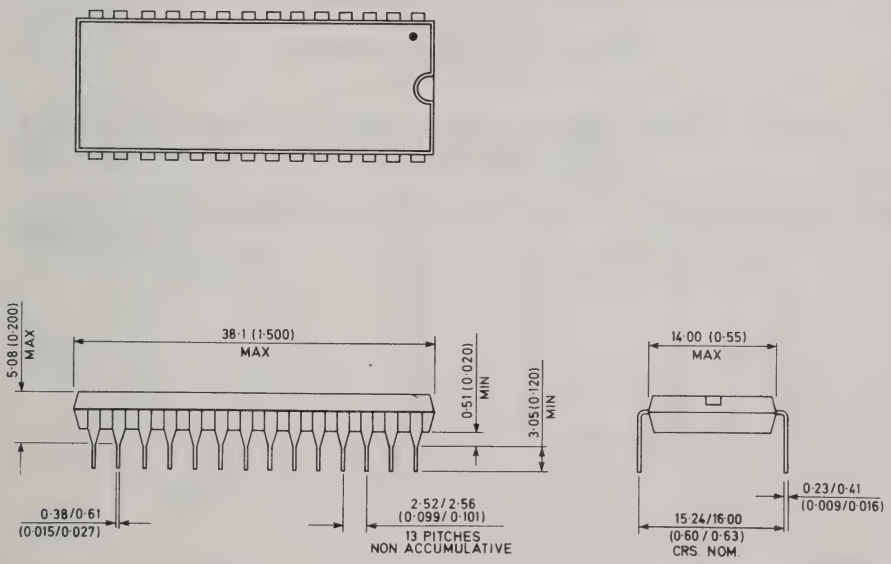

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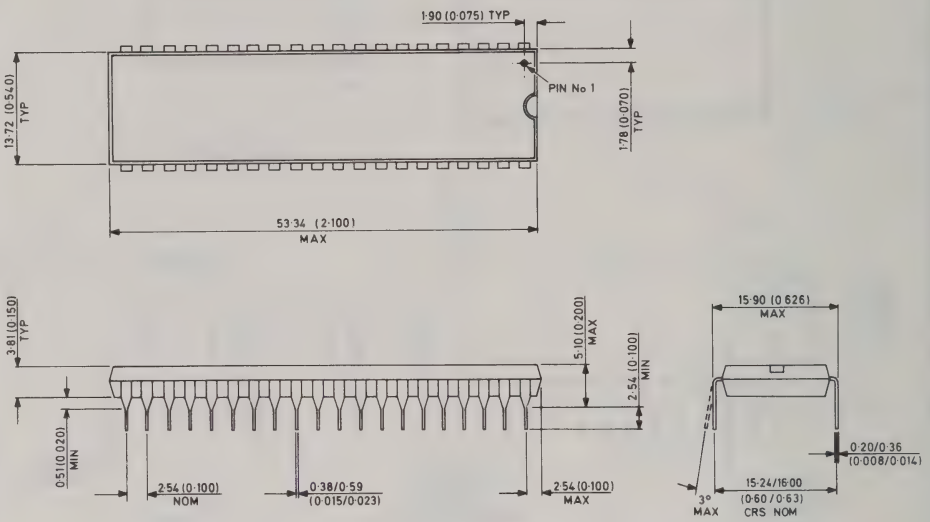

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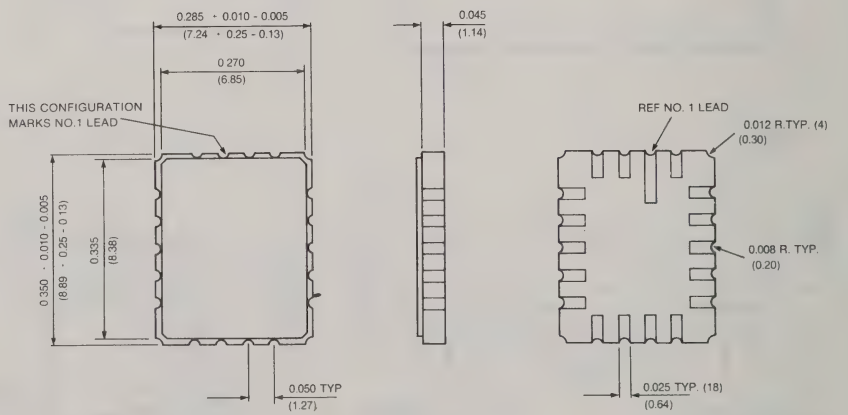

NOTE
Lid connected to pin 9 - Vss

18 LEAD SURFACE MOUNTING PACKAGE **LC18**

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